

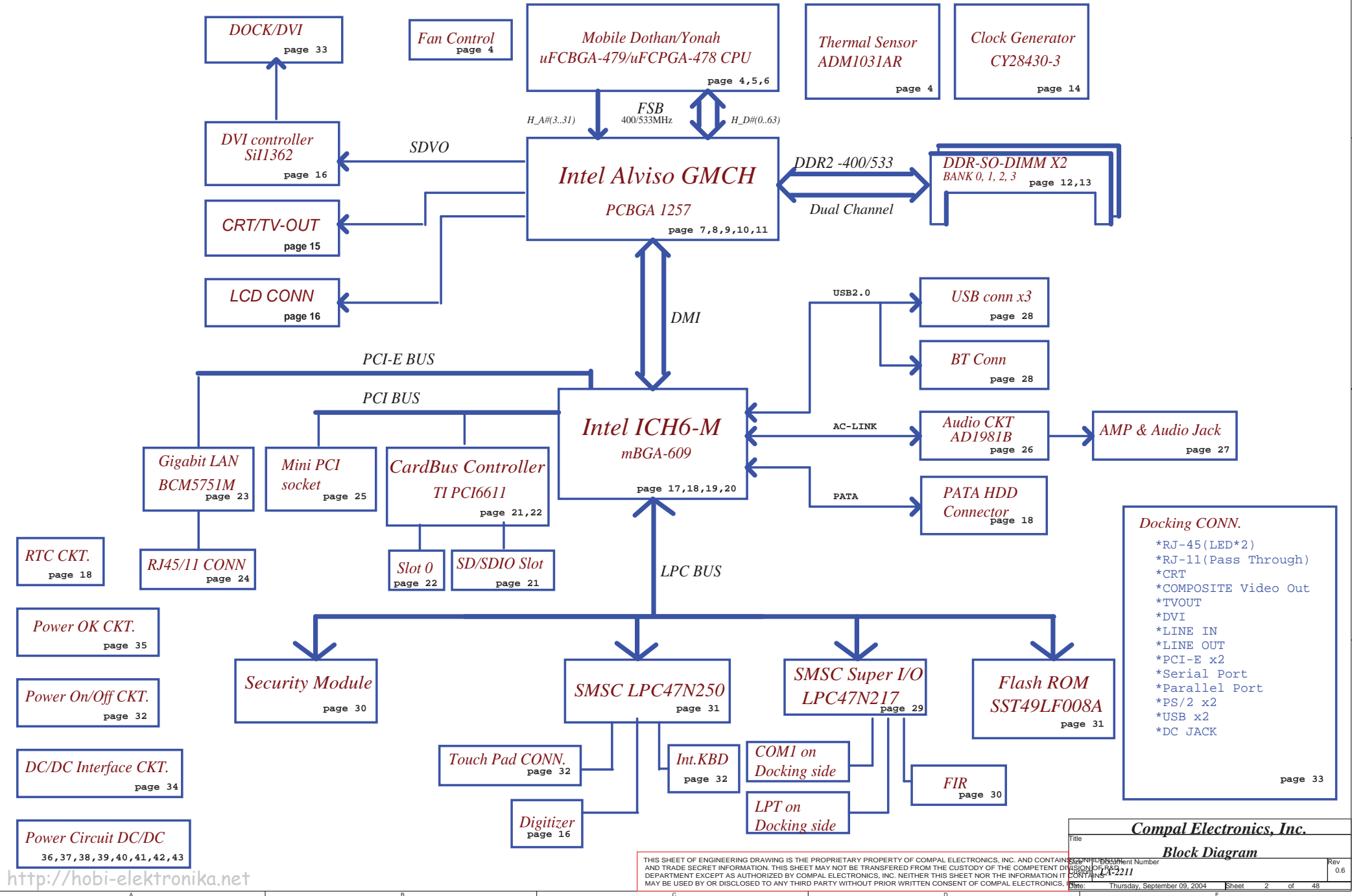
# Compal confidential

## Schematics Document Mobile Dothan uFCBGA/uFCPGA with Intel Alviso\_GM+ICH6-M core logic

2004-09-09

REV:06

# Heavenly





Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12Vswitched power rail on power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol note:

-  :means digital ground.
-  :means analog ground.
- @ :means reserved.

Internal PCI Devices

DEVICE	PCI Device ID	IDSEL #
LAN	D8	AD24
Azalia	D27	AD11
PCI-E	D28	AD12
USB1.1/2.0	D29	AD13
PCI to PCI (DMI to PCI)	D30	AD14
AC97 MODEM	D30	AD14
AC97 Audio	D30	AD14
PATA/SATA	D31	AD15
LPC I/F	D31	AD15
SMBUS	D31	AD15

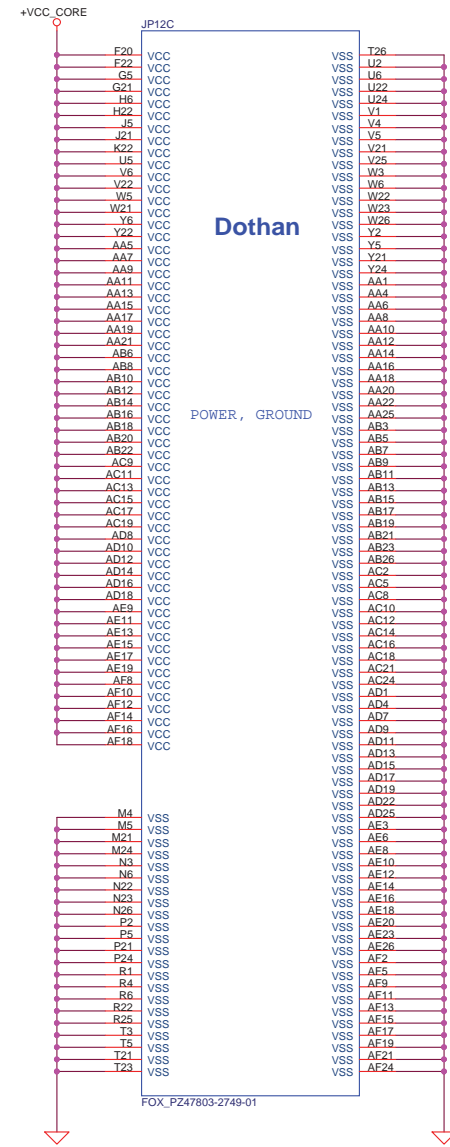
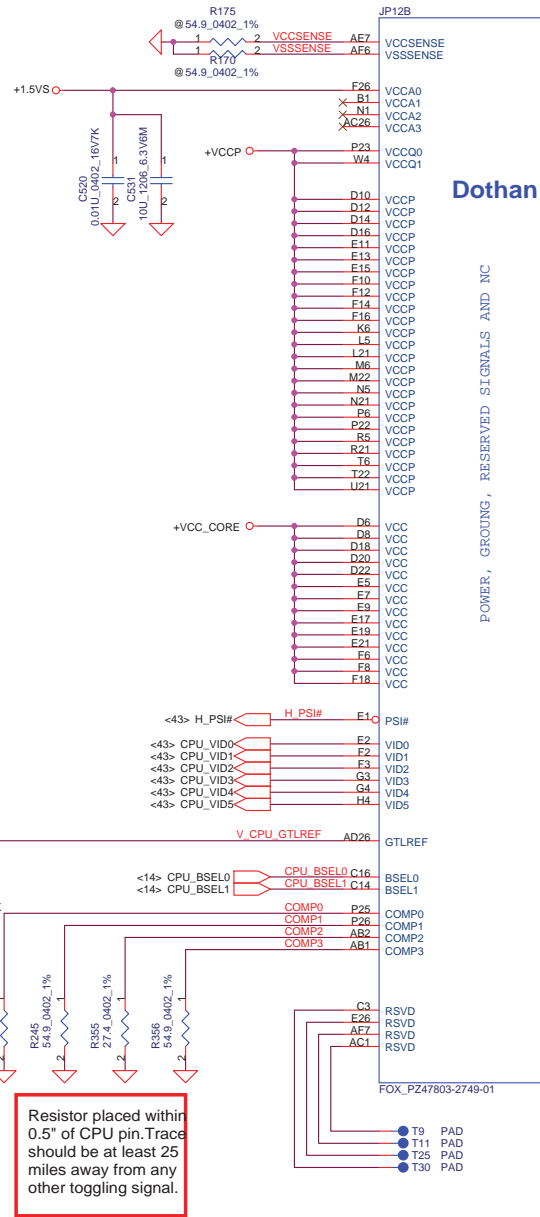
External PCI Devices

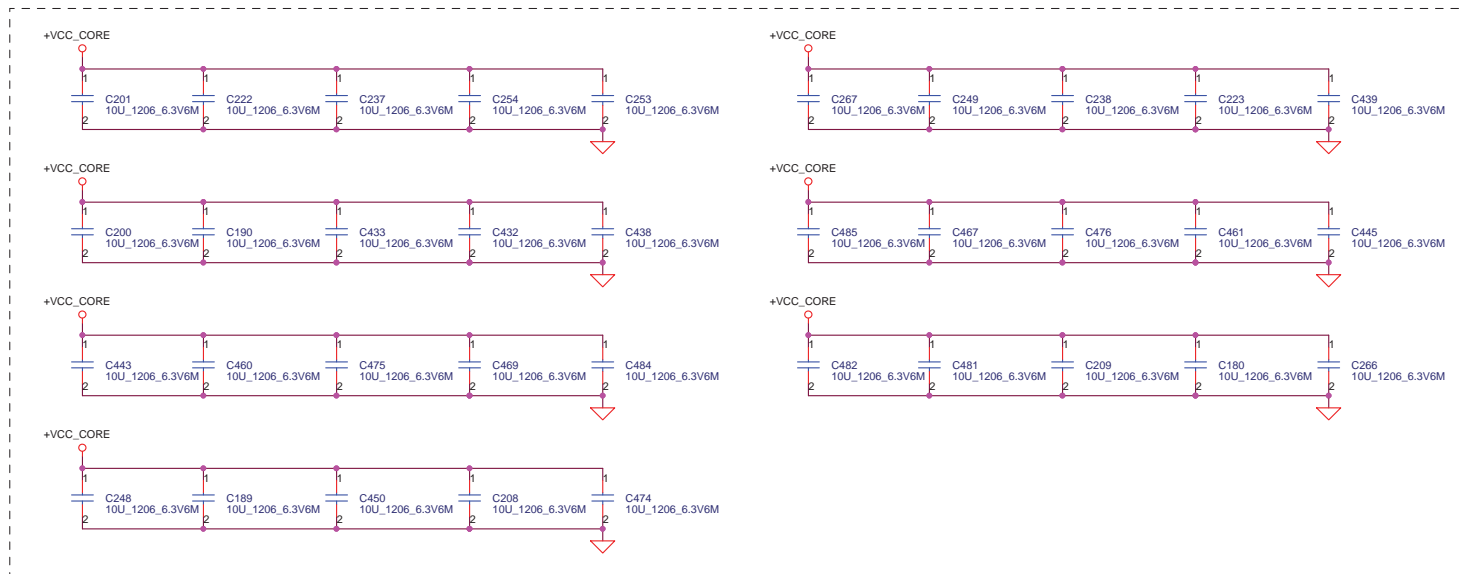
DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
Mini-PCI	D4	AD20	0	F
CARD BUS	D6	AD22	2	A B C D

I2C / SMBUS ADDRESSING

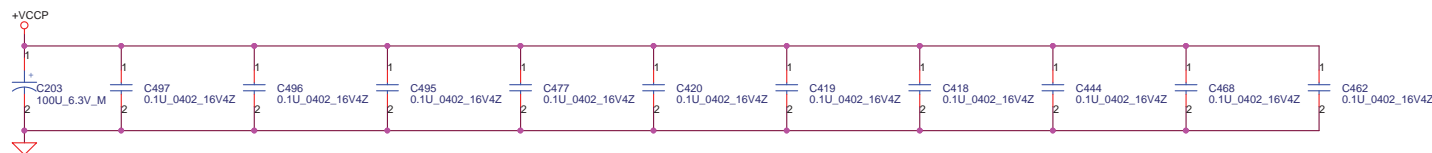
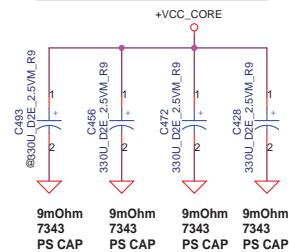
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

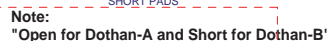
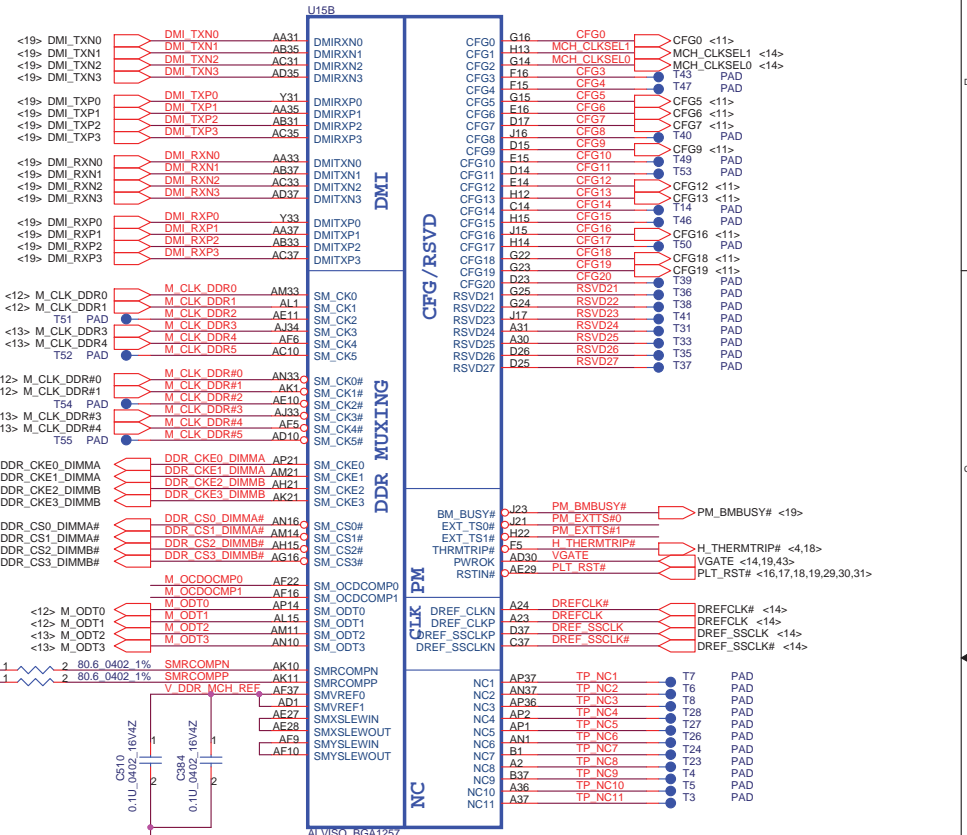


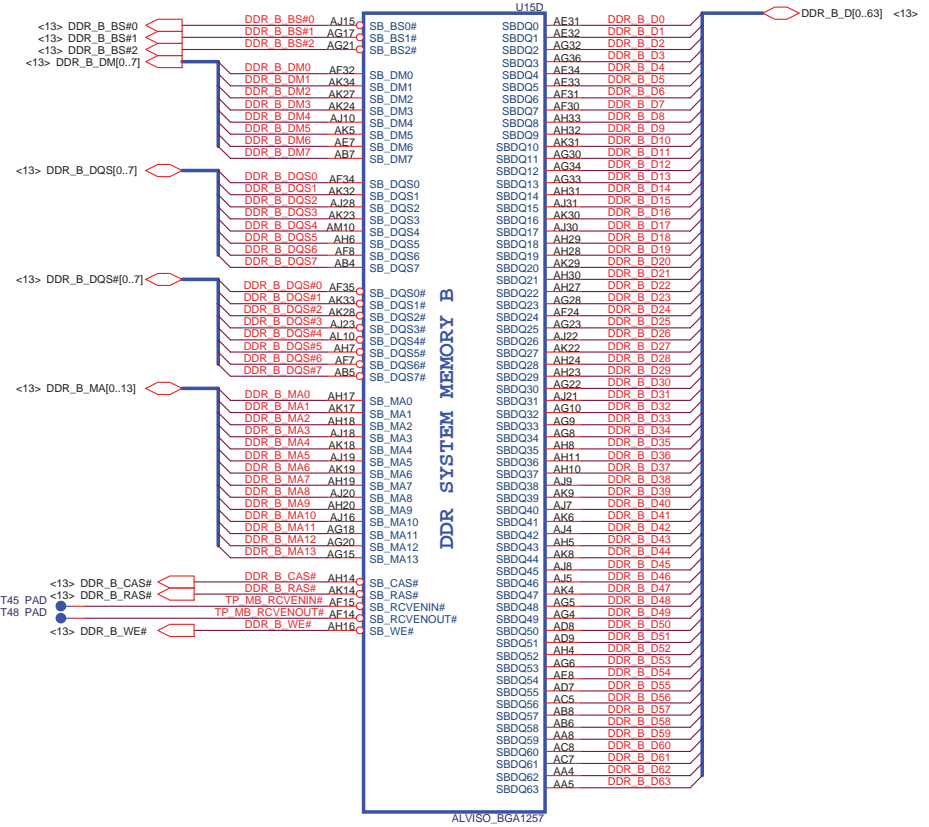
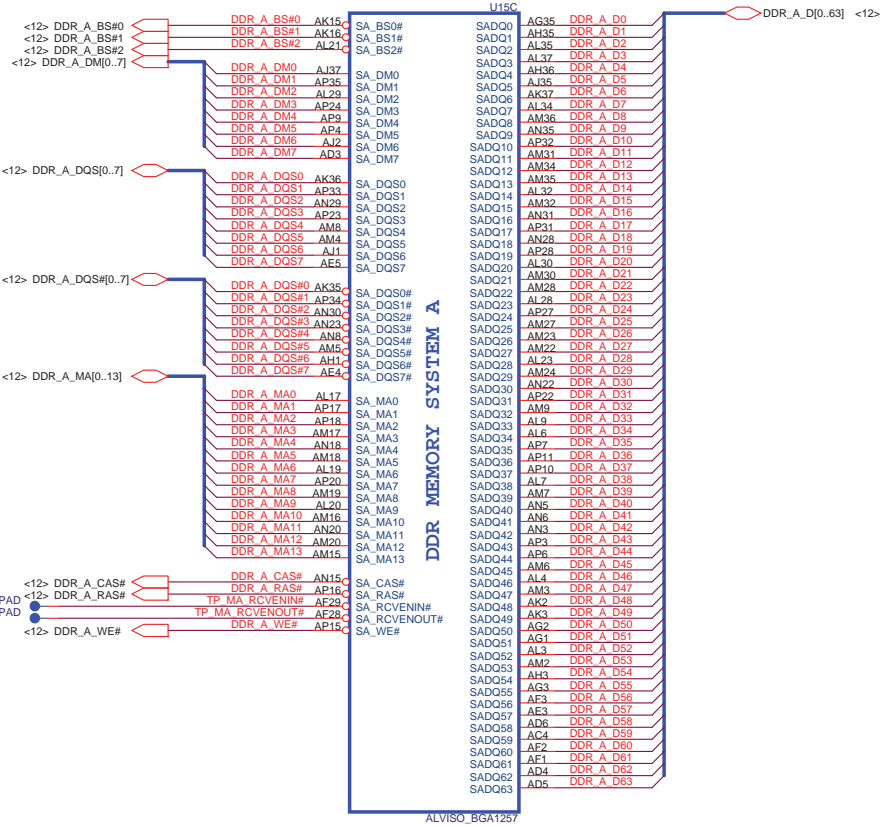




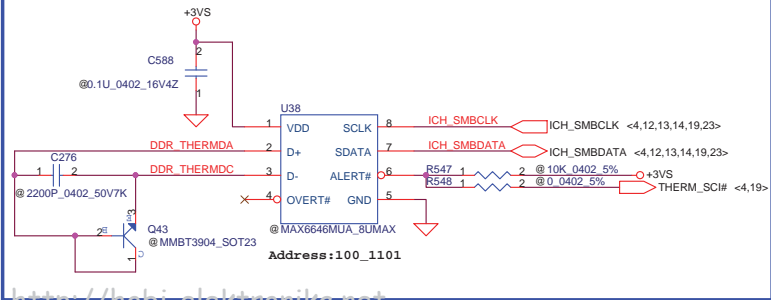
### Near VCORE regulator.



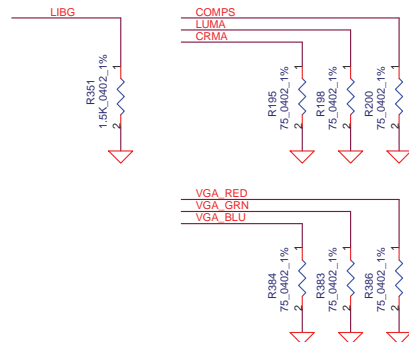
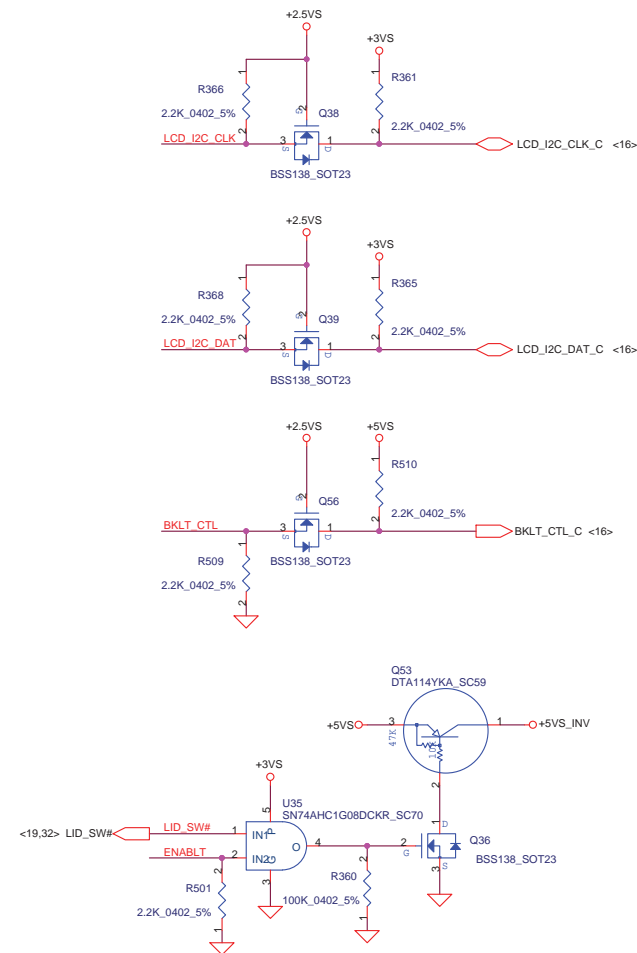
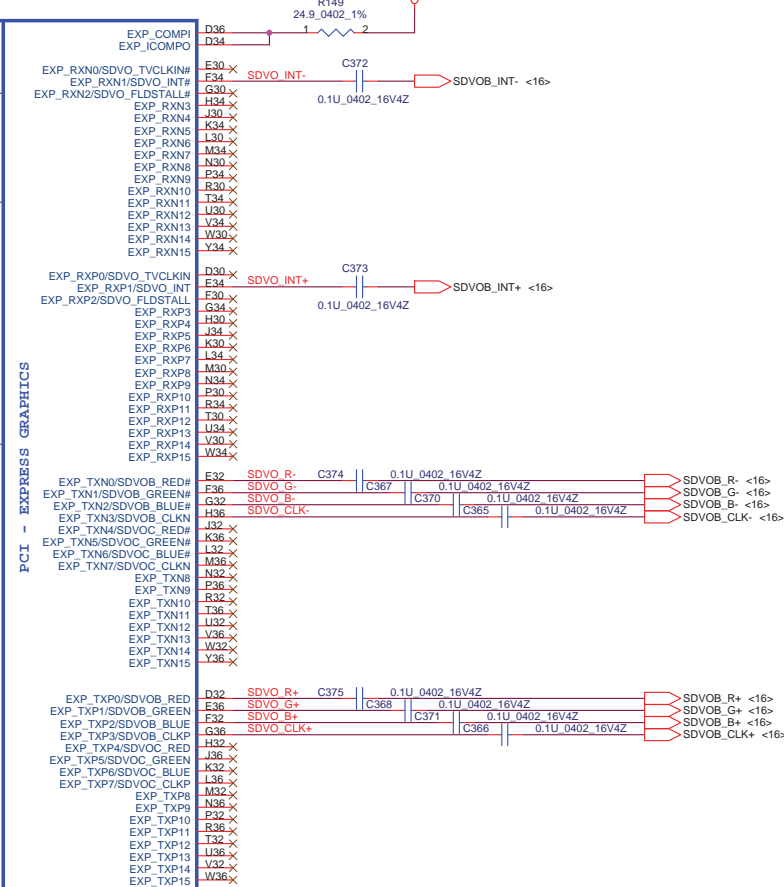
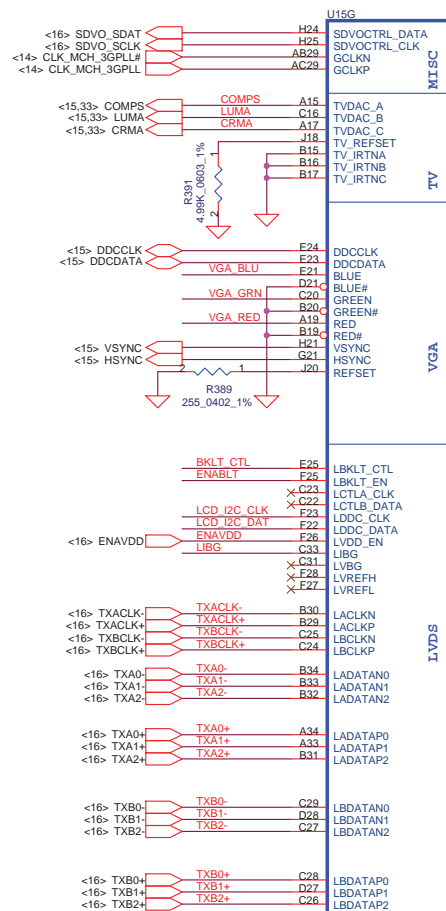




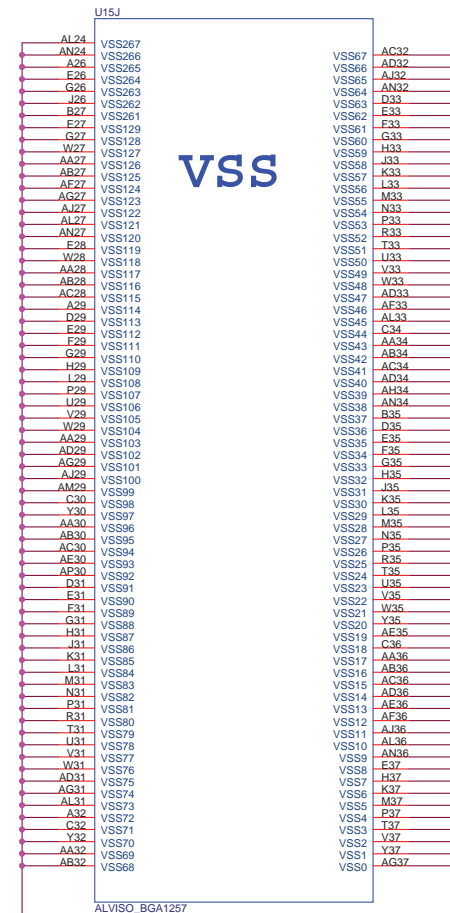
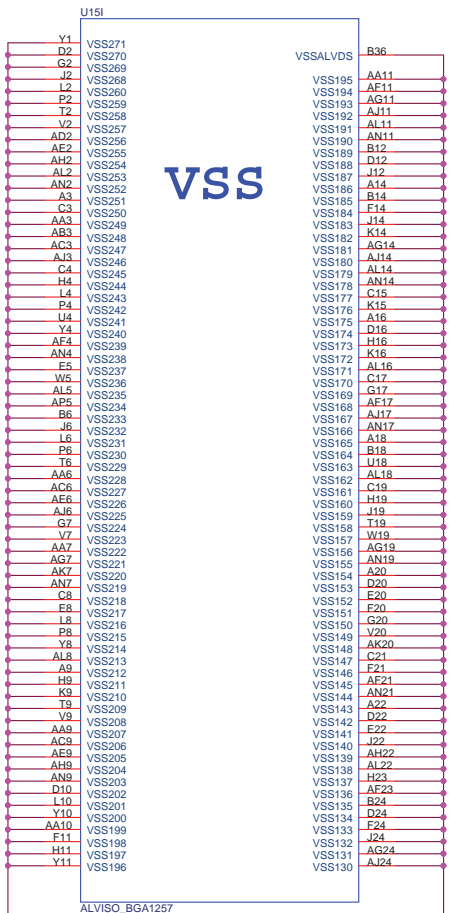
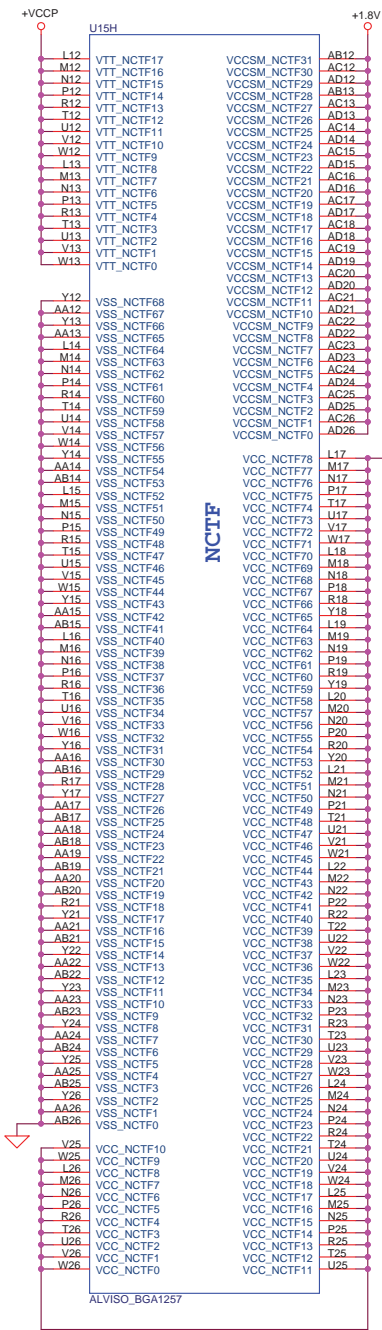
## Reserved thermal CKT and closed to JP34.



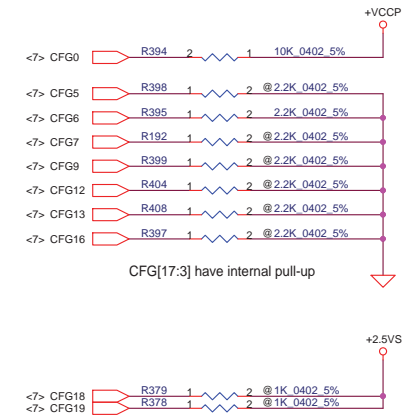


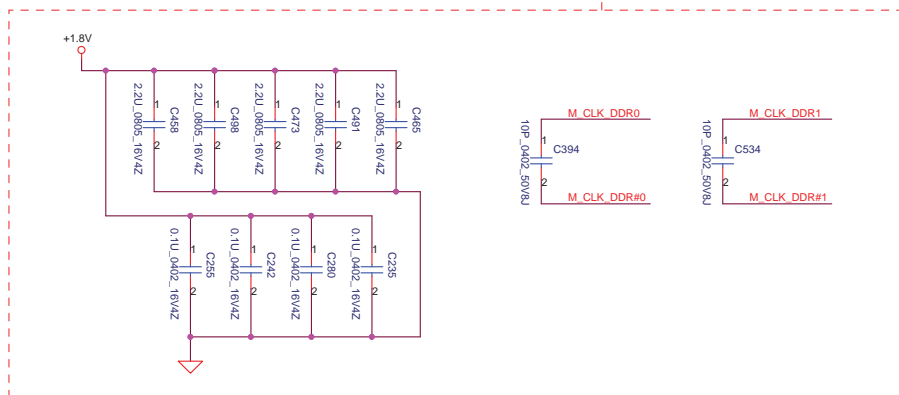
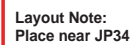




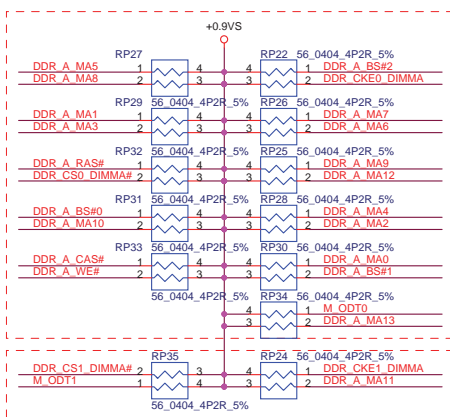
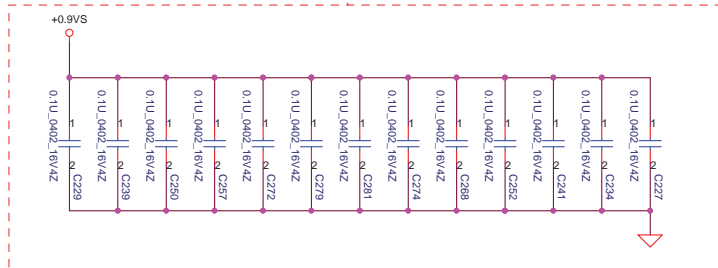


CFG[2:0]	Refer to page14 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II * High = DDR-I
CFG7	Low = DT/Transportable CPU High = Mobile CPU *
CFG9	Low = Reverse Lane High = Normal Operation *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V



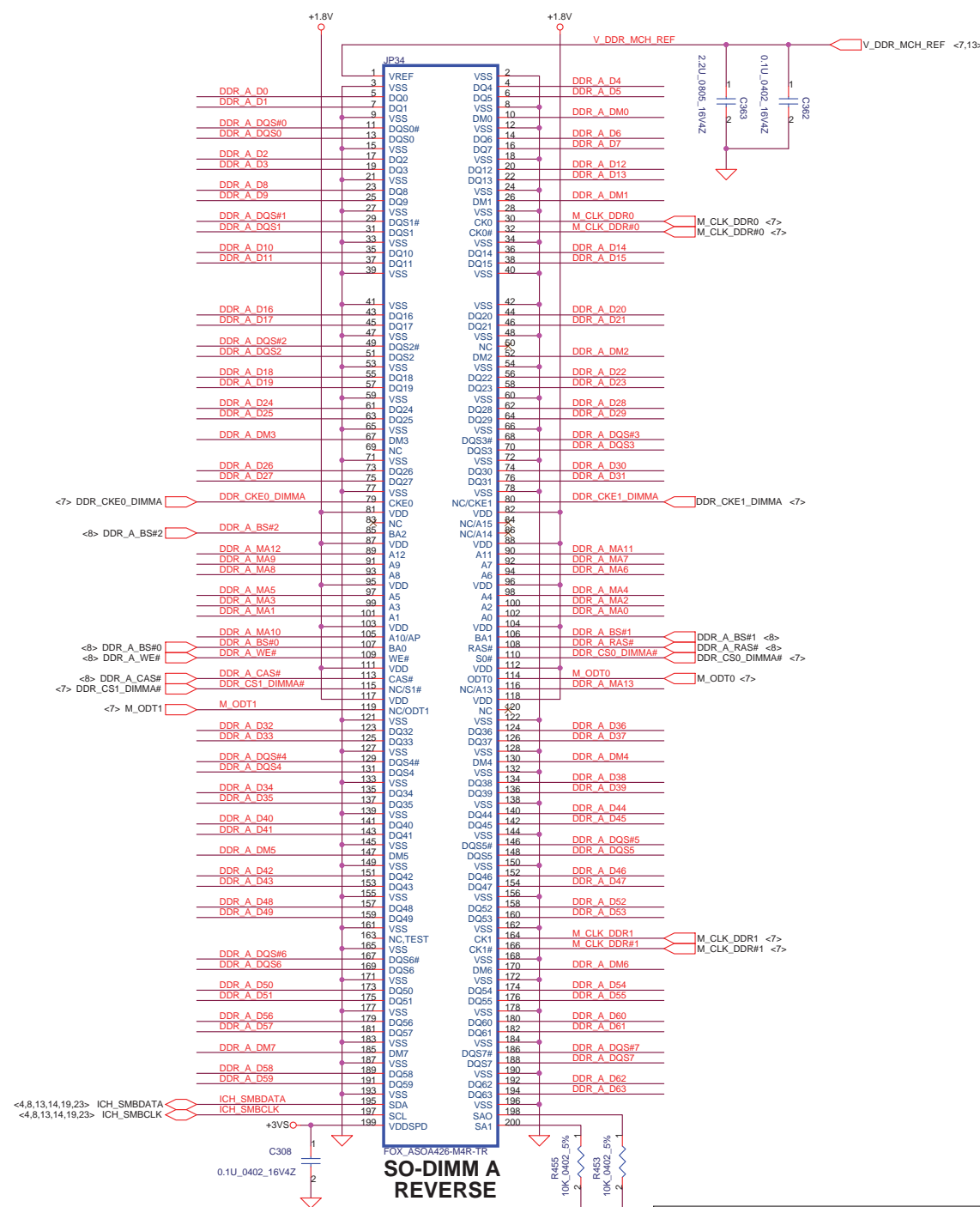


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VT



**Layout Note:**  
Place these resistor  
closely JP34,all  
trace length<750 mil

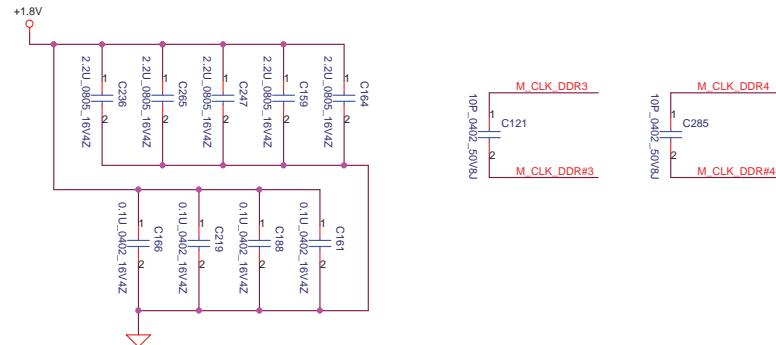
**Layout Note:**  
Place these resistor  
closely JP34,all  
trace length Max=1.3"



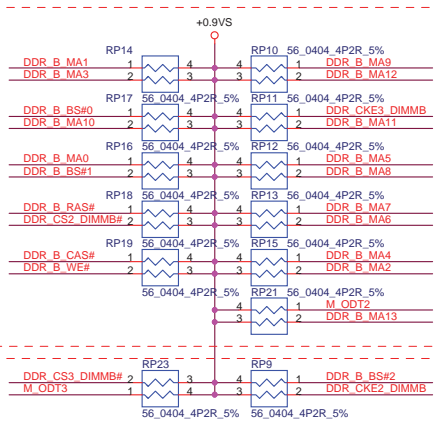
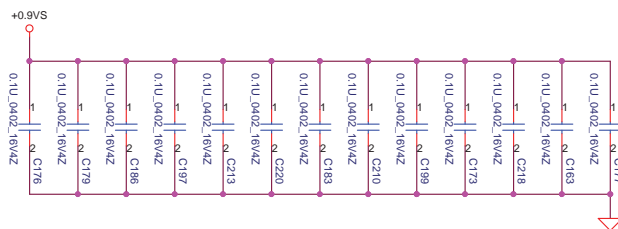
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DATE: 11/11/2004  
 DRAWN BY: J. H. CHEN  
 CHECKED BY: J. H. CHEN  
 APPROVED BY: J. H. CHEN  
 TITLE: DDRII-SODIMM SLIOT1  
 SHEET: 12 OF 48  
 REV: 0.0

**Layout Note:**  
Place near JP10

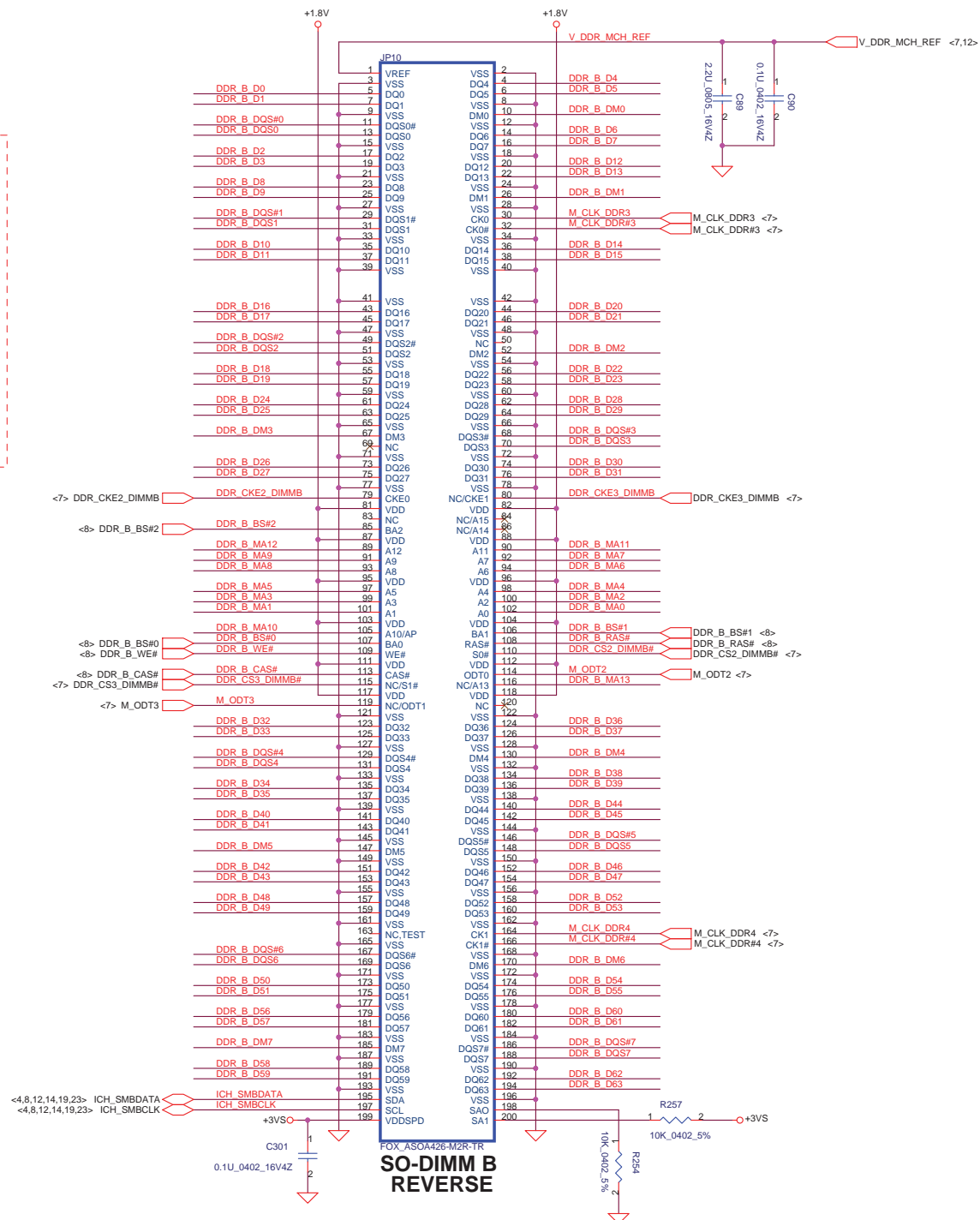


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



**Layout Note:**  
Place these resistor  
closely JP10,all  
trace length<750 mil

**Layout Note:**  
Place these resistor  
closely JP10,all



**SO-DIMM E  
REVERSE**

Title **Compal Electronics, Inc.**  
**DDRII-SODIMM SLOT2**

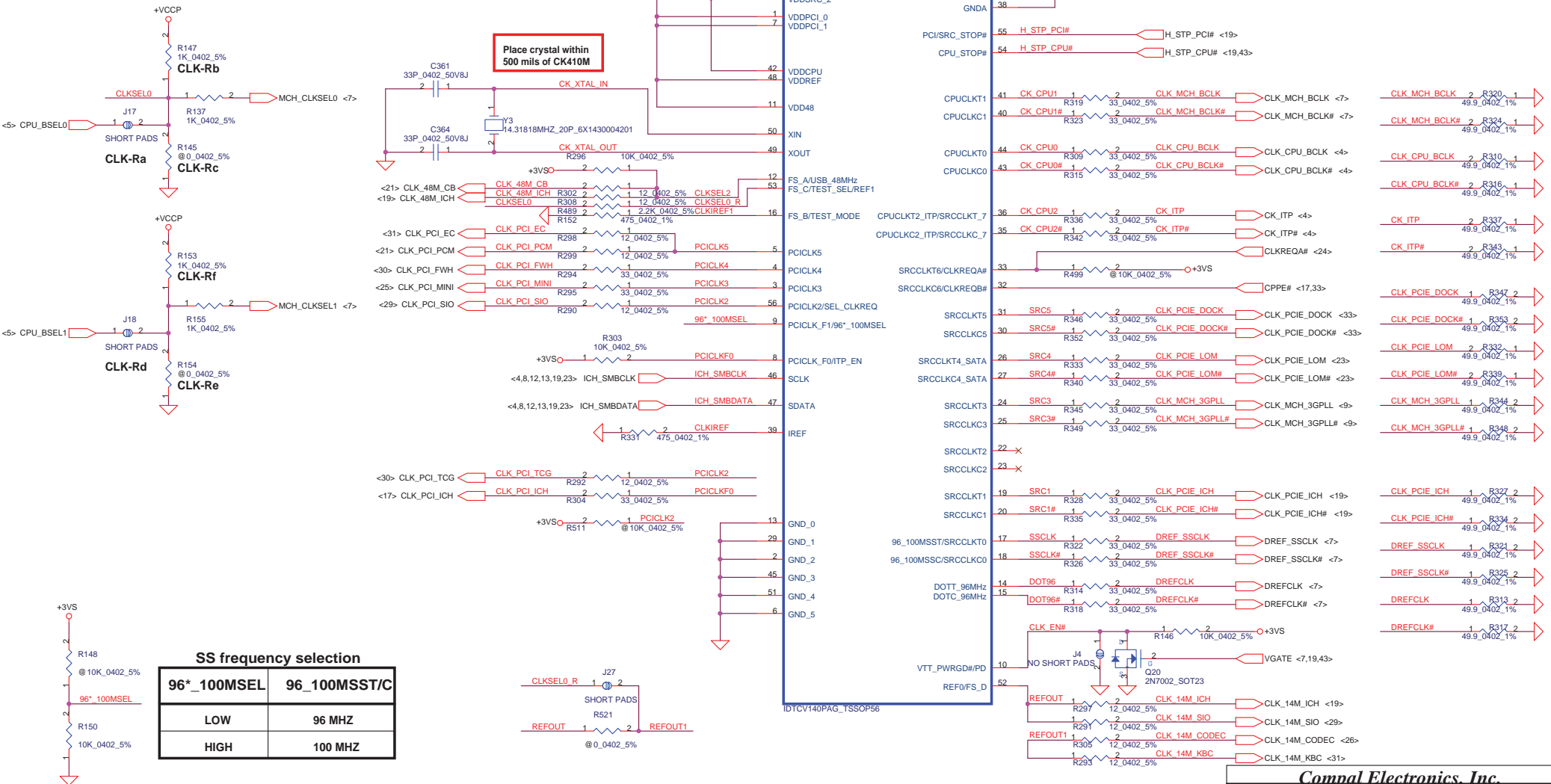
REGION OF ORIGIN CONTAINS LA-2211		Revision Number Rev 0.6
Date:	Thursday, September 09, 2004	Sheet 13 of 48

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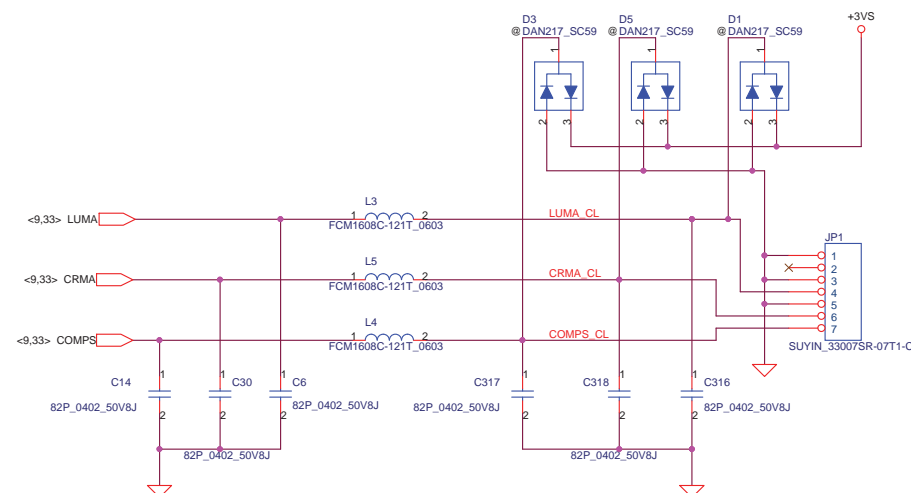
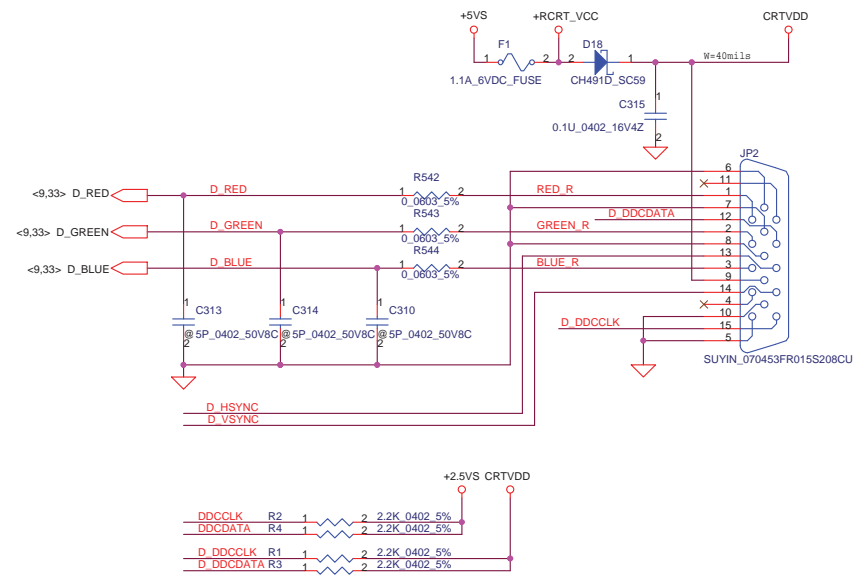


FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
1	0	1	100	100	33.3

CPU Type	CLK-Ra	CLK-Rb	CLK-Rc	CLK-Rd	CLK-Re	CLK-Rf
Dothan-A PSB400	OPEN	1K Ohm	OPEN	OPEN	0 Ohm	OPEN
Dothan-A PSB533	OPEN	OPEN	0 Ohm	OPEN	0 Ohm	OPEN
Dothan-B	SHORT	1K Ohm	OPEN	0 Ohm	OPEN	1K Ohm



## TV-Out Connector



## LCD POWER CIRCUIT

The LCD POWER CIRCUIT schematic shows the power regulation for the LCD. It includes a +5VALW input connected to a network of resistors (R19, R12) and capacitors (C29, C31, C20, C28). Transistors Q5, Q6, and Q8 are used for switching and regulation. The output is LCDVDD. A signal ENAVDD is also shown.

## LCD/PANEL BD. CONN.

The LCD/PANEL BD. CONN. schematic shows the connection between the LCD/PANEL board and the main board. It includes connectors J8, J9, J28, and various signal lines like DIGI TX, DIGI RX, DIGI RESET#, ALS EN, LCD I2C CLK C, LCD I2C DAT C, KSI D 8, KSI D 9, KSI D 10, KSI D 11, KSO14, TXBCLK-, TXBCLK+, TXB0-, TXB0+, TXB1-, TXB1+, TXB2-, TXB2+, TXACLK-, TXACLK+, TXA2-, TXA2+, TXA1-, TXA1+, TXA0-, TXA0+.

## DVI CONTROLLER

The DVI CONTROLLER schematic shows the connection between the DVI controller (U11) and the DVI port. It includes resistors R497, R103, R107, R498, and capacitors C115, C104, C123, C358, C359, C360. Input signals include DVI AVDD 3V, DVI DVDD 2.5V, DVI CLK-, DVI CLK+, DVI TX0-, DVI TX0+, DVI TX1-, DVI TX1+, DVI TX2-, DVI TX2+, DVI DETECT, DVI DDC CLK, DVI DDC DAT, SDVO SDAT, SDVO SCLK, SDVO INT+, SDVO INT-, SDVOB\_R+, SDVOB\_R-, SDVOB\_G+, SDVOB\_G-, SDVOB\_B+, SDVOB\_B-, SDVOB\_CLK+, SDVOB\_CLK-.

The DVI CONTROLLER schematic shows the connection between the DVI controller (U11) and the DVI port. It includes resistors R131, R132, R301, R300, and capacitors C115, C104, C123, C358, C359, C360. Input signals include DVI AVDD 3V, DVI DVDD 2.5V, DVI CLK-, DVI CLK+, DVI TX0-, DVI TX0+, DVI TX1-, DVI TX1+, DVI TX2-, DVI TX2+, DVI DETECT, DVI DDC CLK, DVI DDC DAT, SDVO SDAT, SDVO SCLK, SDVO INT+, SDVO INT-, SDVOB\_R+, SDVOB\_R-, SDVOB\_G+, SDVOB\_G-, SDVOB\_B+, SDVOB\_B-, SDVOB\_CLK+, SDVOB\_CLK-.

Compal Electronics, Inc.			
DVI (Si1362)/LCD CONN.			
File	Revision	Sheet	16 of 48
Thursday, September 09, 2004	0.6		

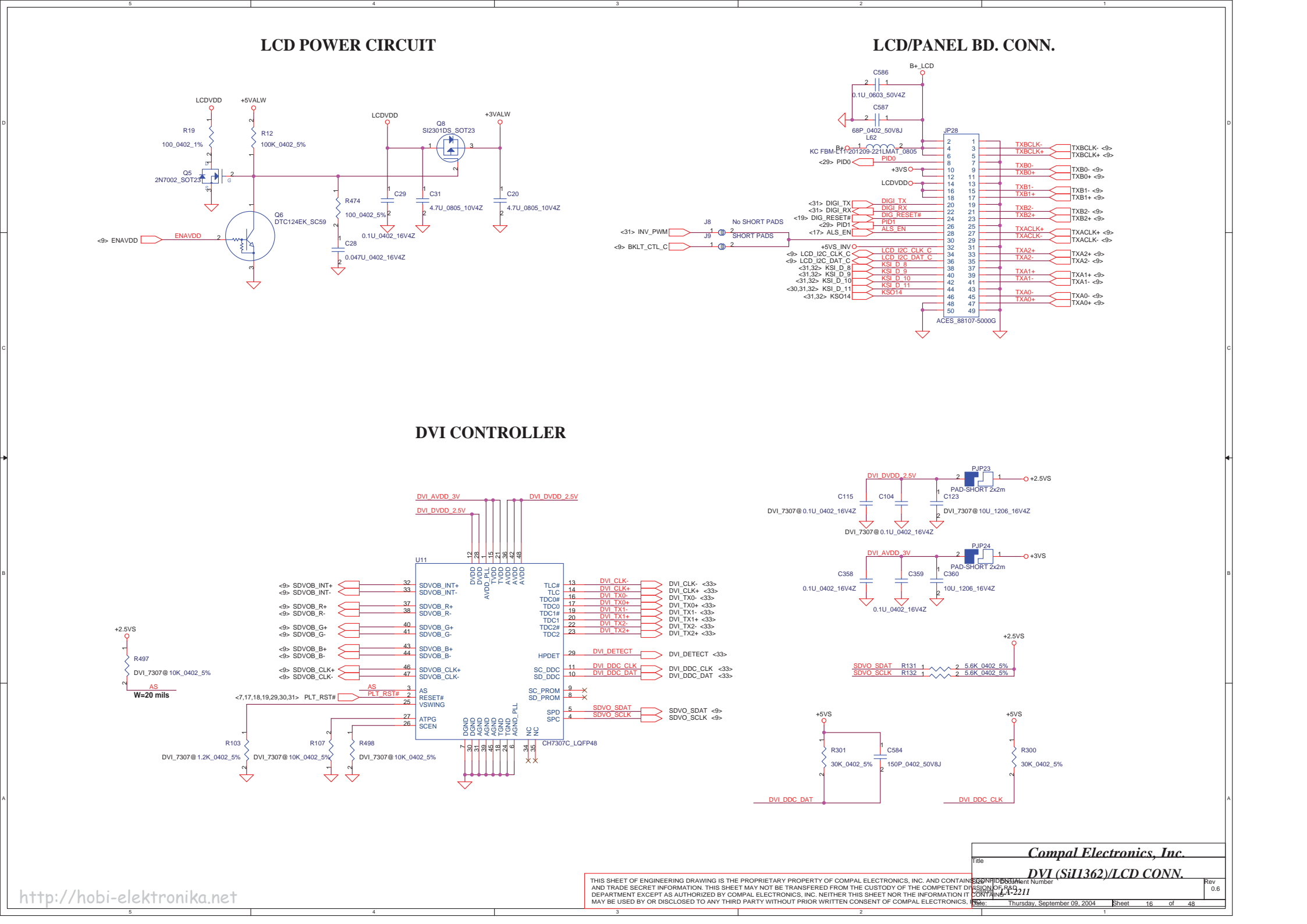
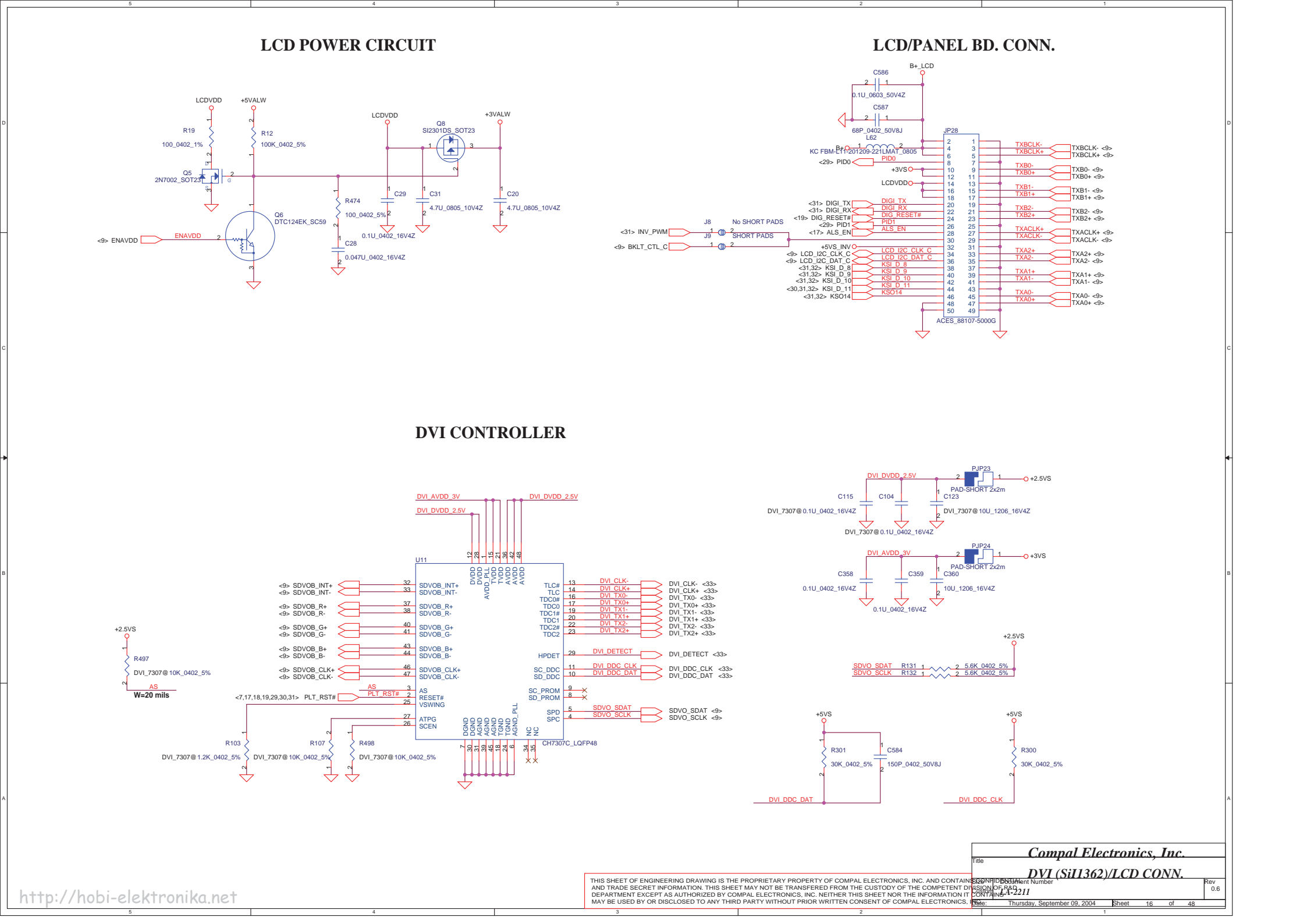
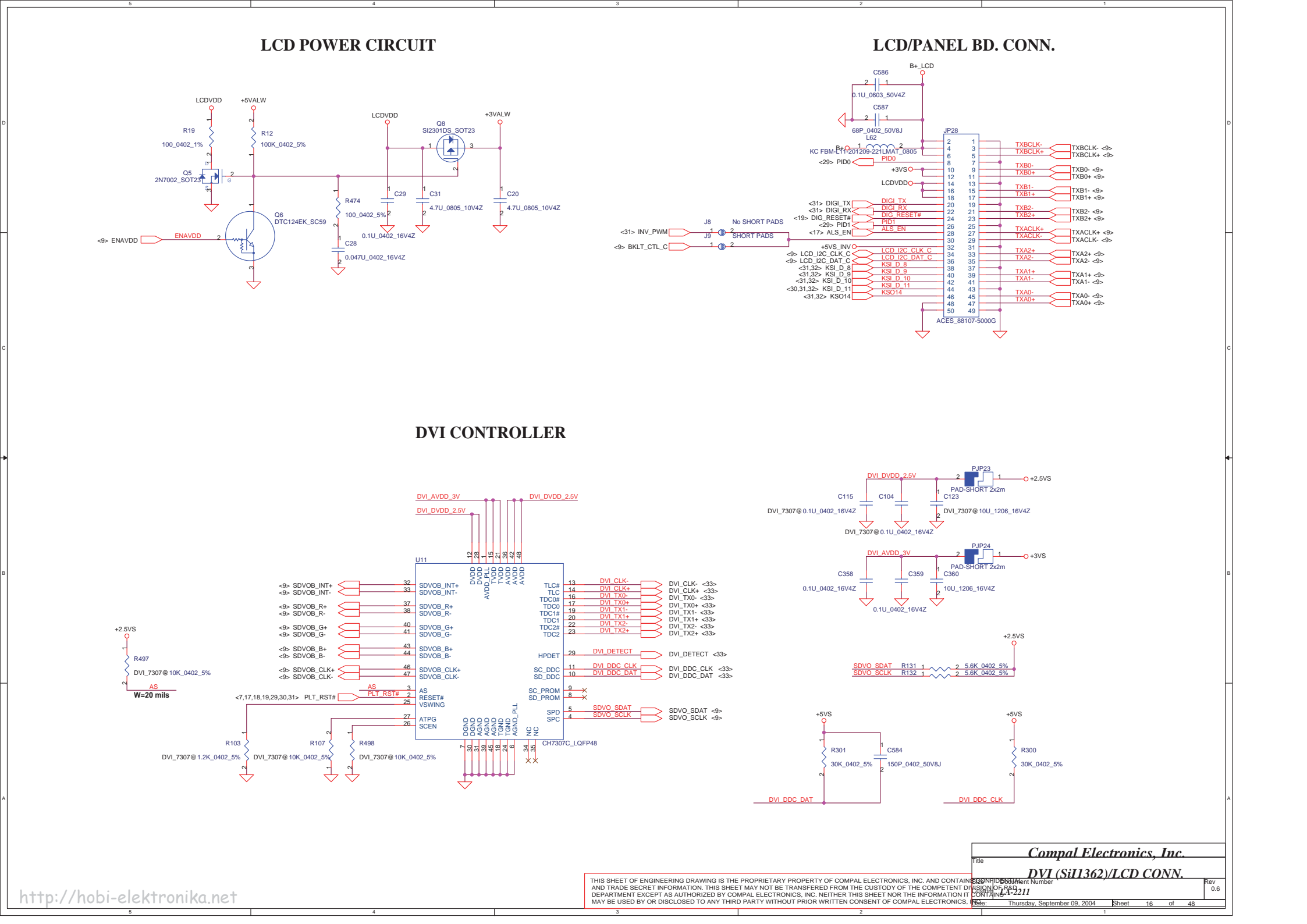
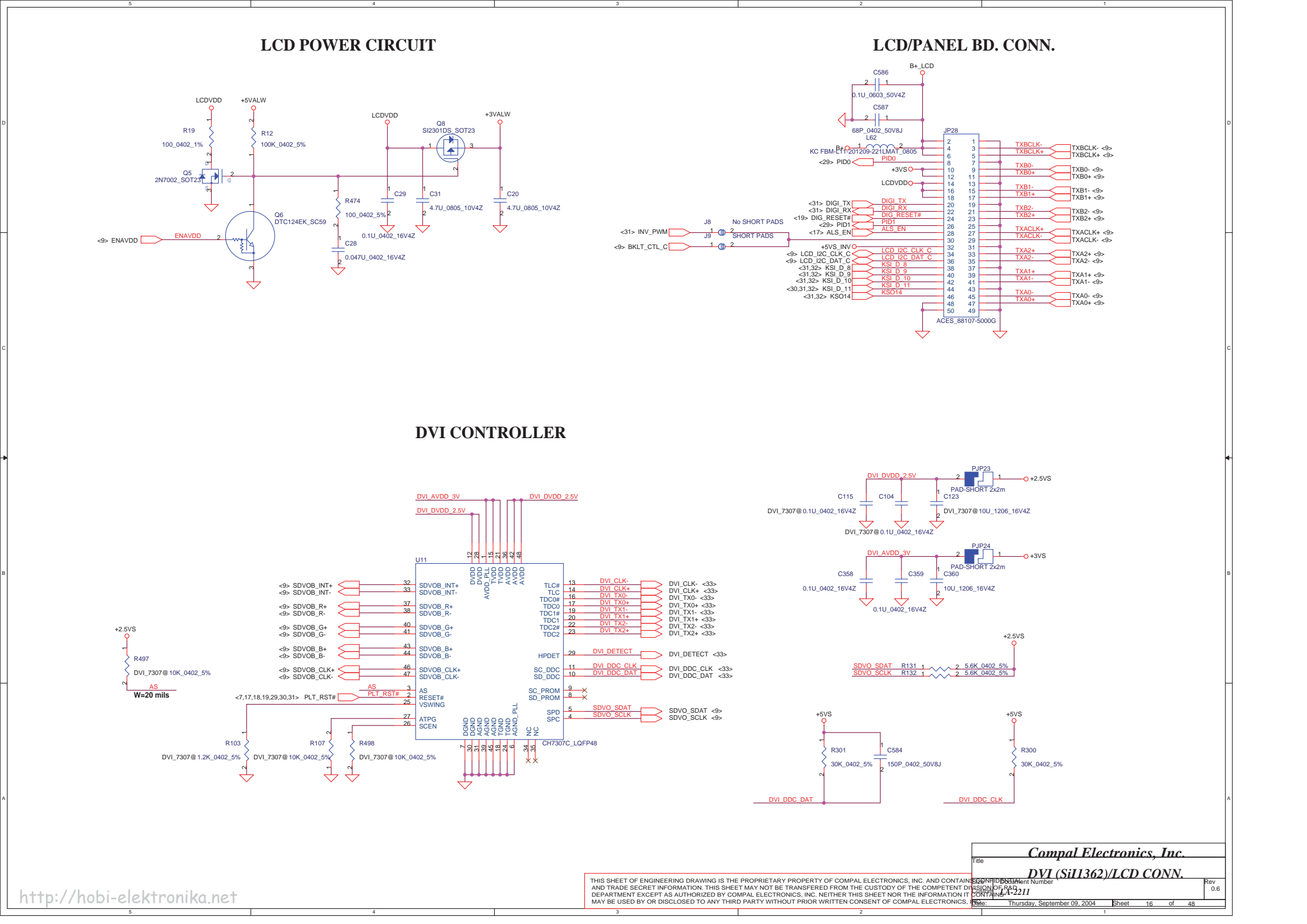
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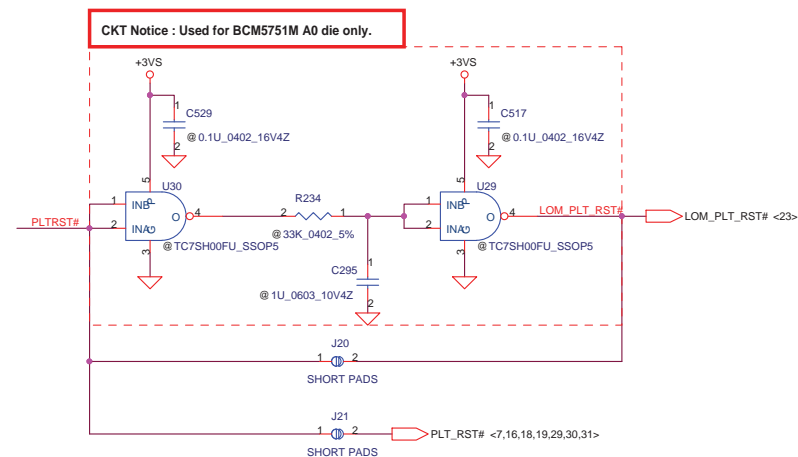
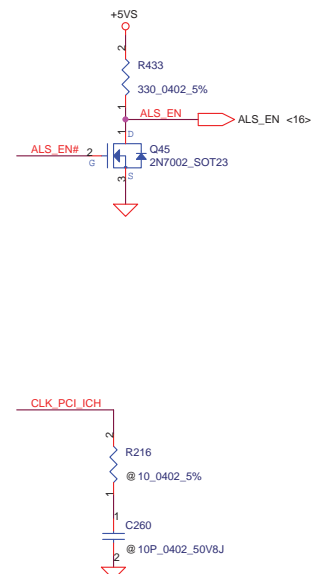
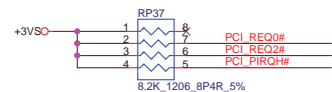
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## LCD POWER CIRCUIT

## LCD/PANEL BD. CONN.



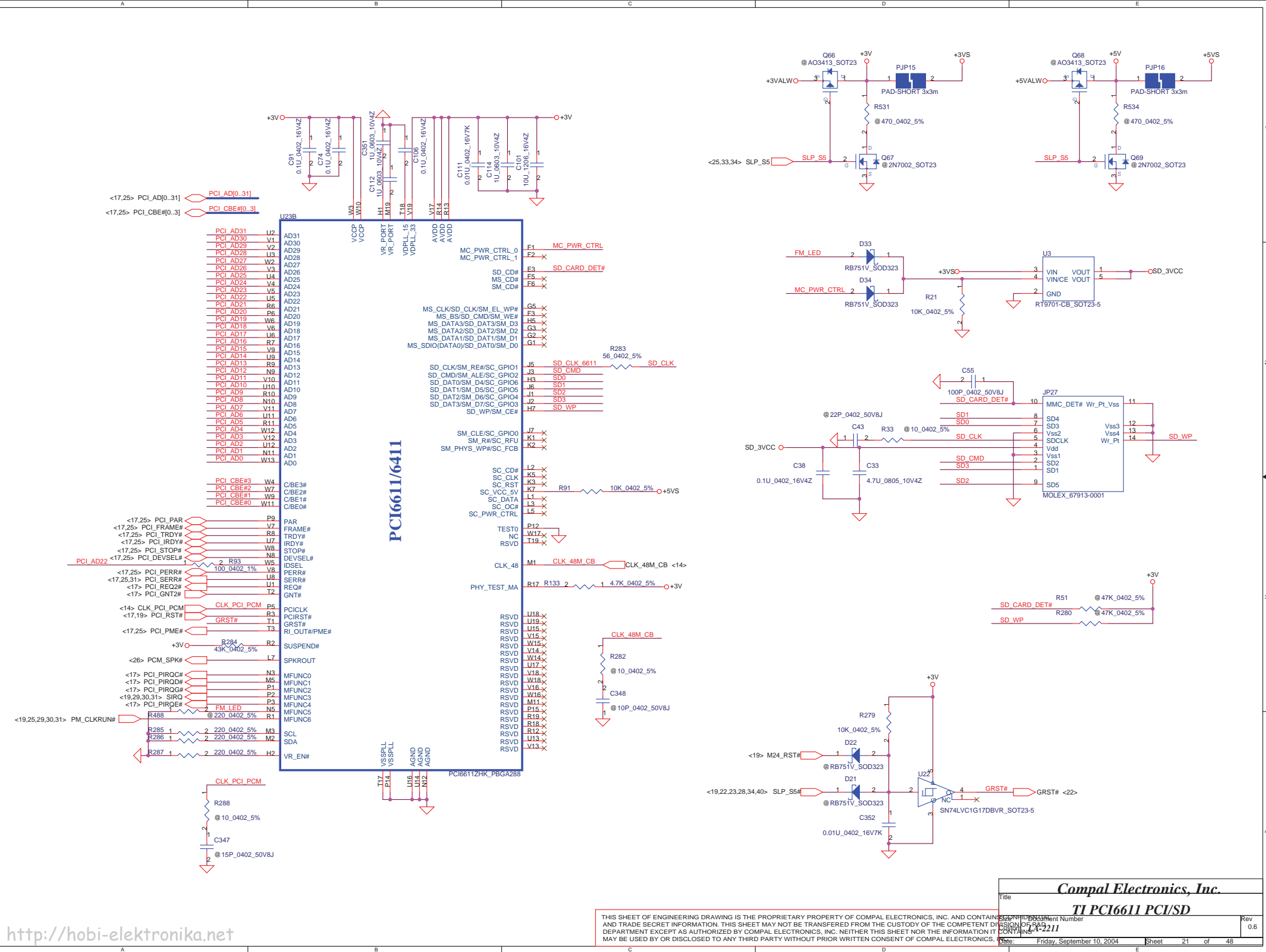


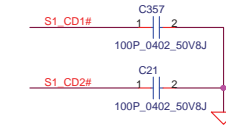
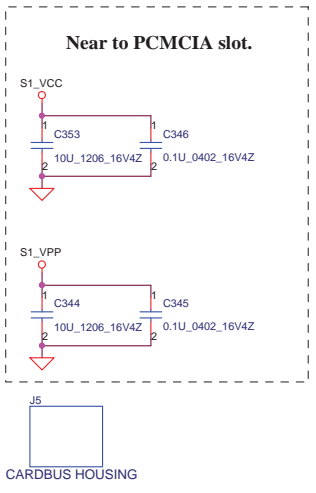
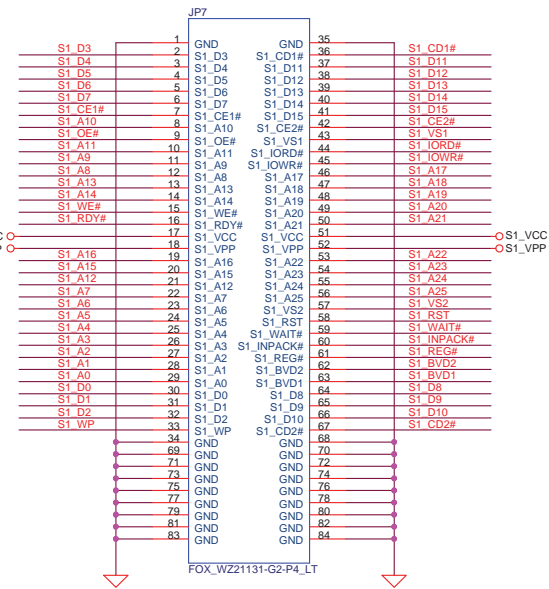




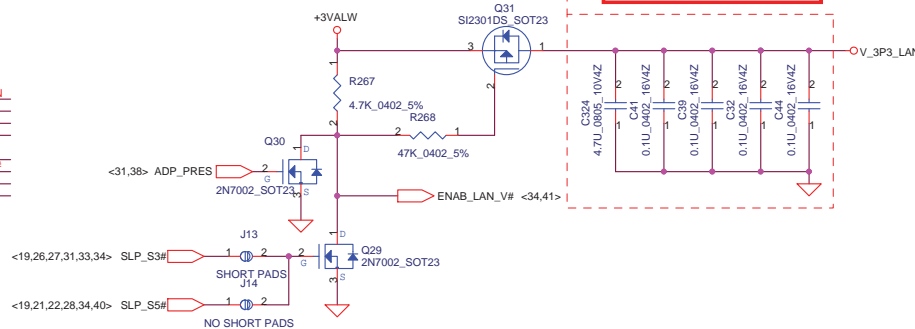
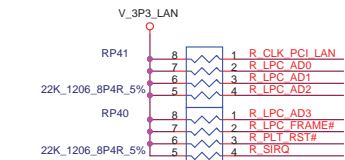








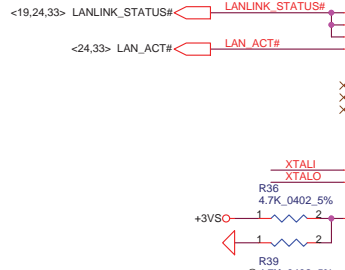
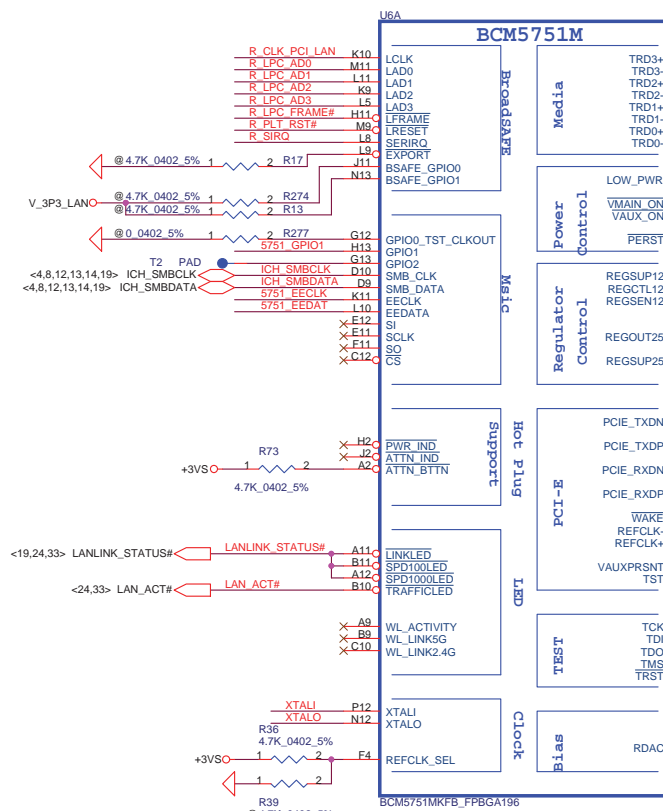




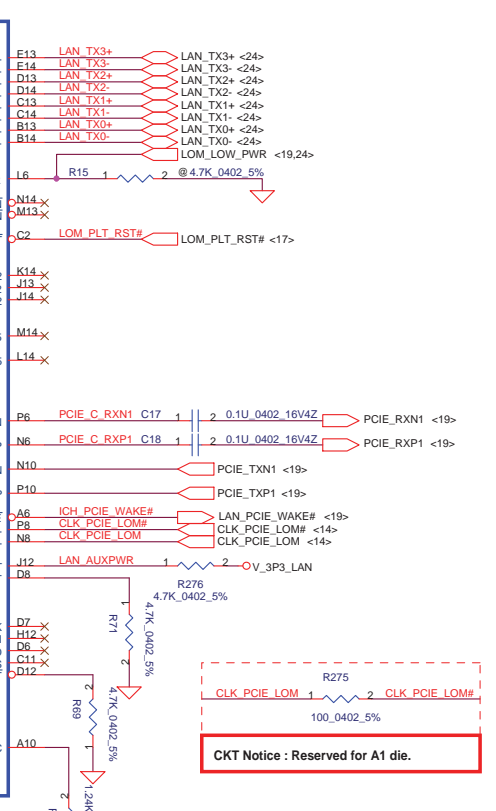
Layout Notice : Place as close chip as possible.

Layout Notice : 3.3V filter. Place as close chip as possible.

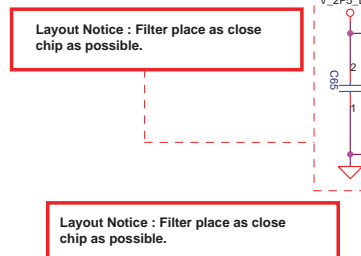
Layout Notice : 1.2V filter. Place as close chip as possible.



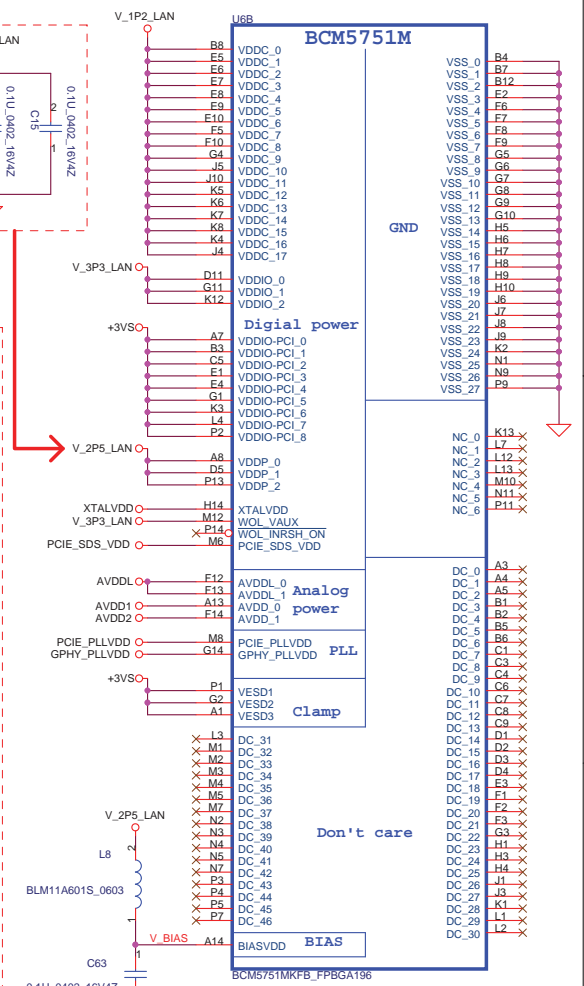
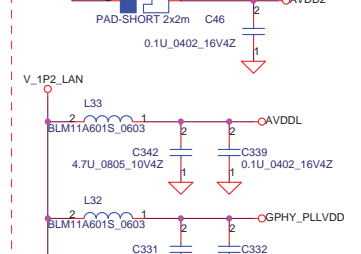
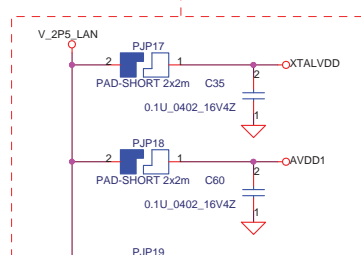
Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC

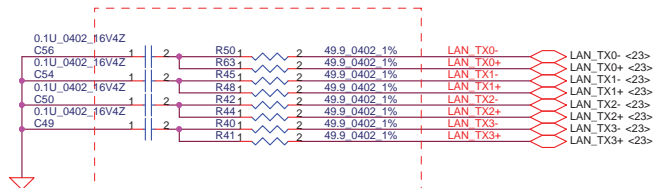


CKT Notice : Reserved for A1 die.



Layout Notice : Filter place as close chip as possible.



[illegible]

Pinout diagram for the FOX\_JM36113-P1121-7F connector. The diagram shows a 14-pin connector with pins 1 through 14. Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, and 14 are labeled with their respective functions and pin numbers. The functions include LANLINK\_STATUS#, MD03-, MD03+, MD01-, MD02-, MD02+, MD01+, MD00-, MD00+, LAN\_ACT#, and LANLINK\_STATUS#. The diagram also shows the internal wiring of the connector, including the MD03- and MD03+ lines, and the MD01- and MD02- lines. The connector is labeled FOX\_JM36113-P1121-7F.

Pin	Function
14	LANLINK_STATUS#
13	Green LED-
12	Green LED+
8	MD03-
7	MD03+
6	MD01-
5	MD02-
4	MD02+
3	MD01+
2	MD00-
1	MD00+
12	LAN_ACT#
11	LANLINK_STATUS#

FOX\_JM36113-P1121-7F

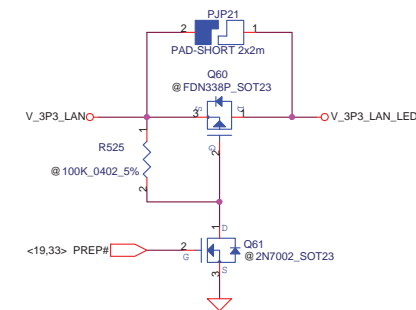
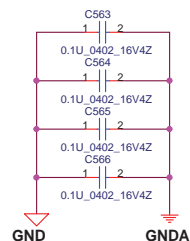
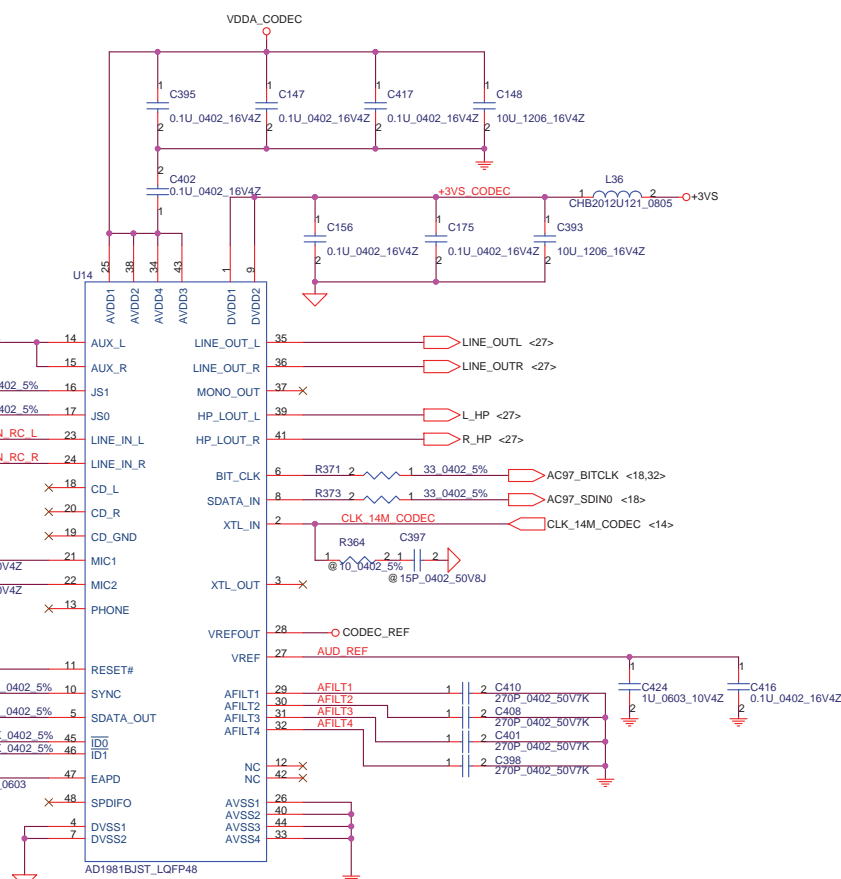
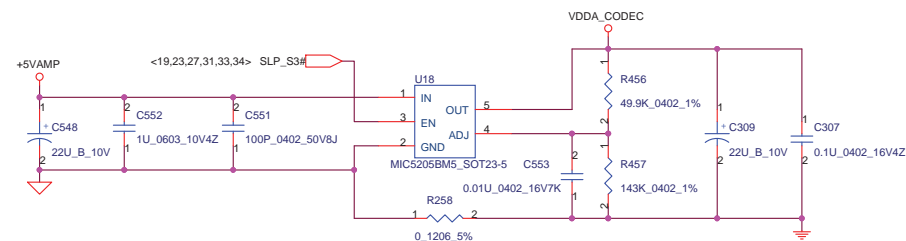


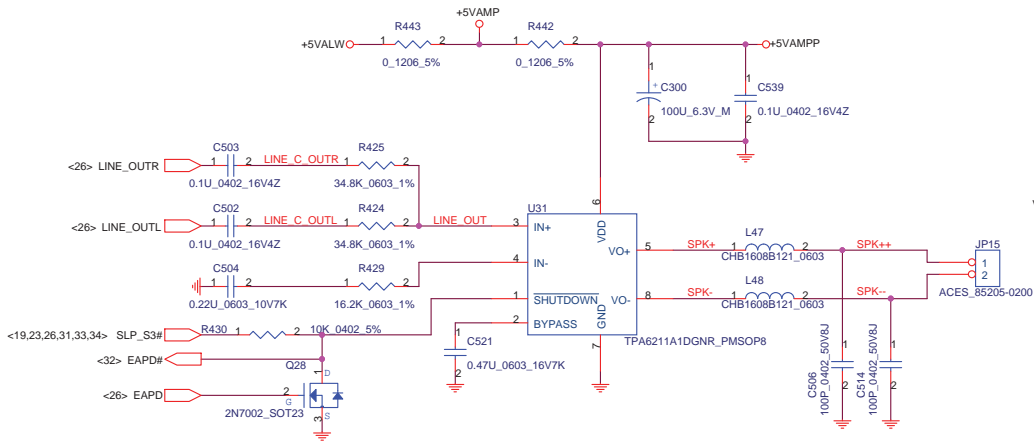
Diagram showing the connection of the MOD TIP and MOD RING signals to the JP4 connector. The MOD TIP signal is connected to pin 1 (TIP) and the MOD RING signal is connected to pin 2 (RING). Pins 3 (GND) and 4 (GND) are also shown, with a ground symbol connected to pin 3. The connector is labeled JP4 and the component is identified as ALLTOP\_C10134-10204.



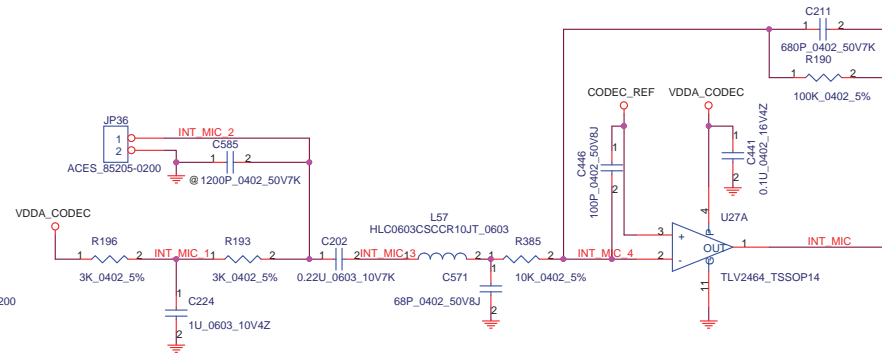




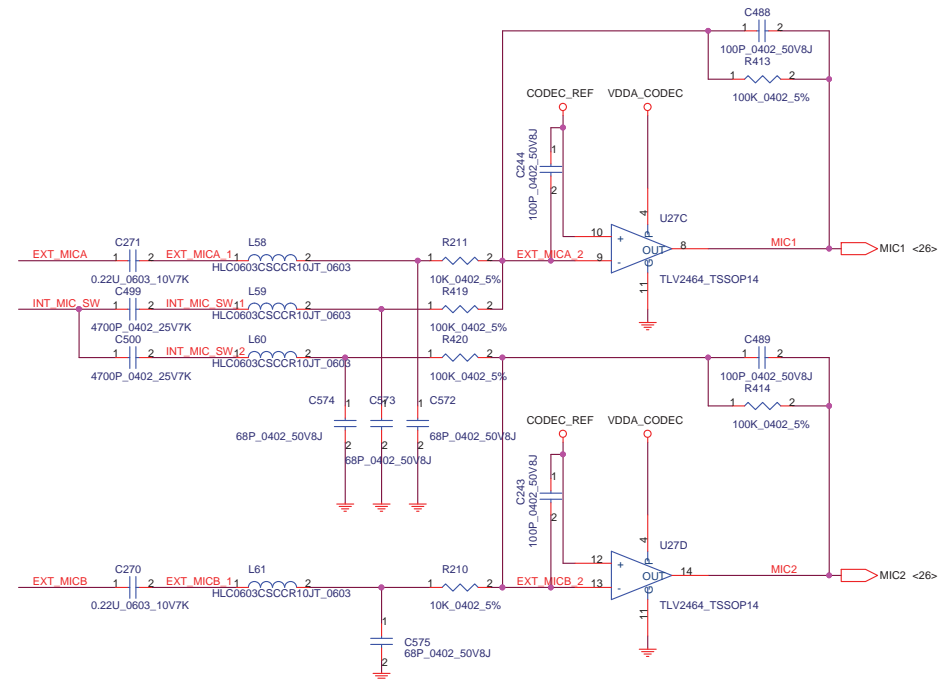
## AMP. FOR INTERNAL SPEAKER



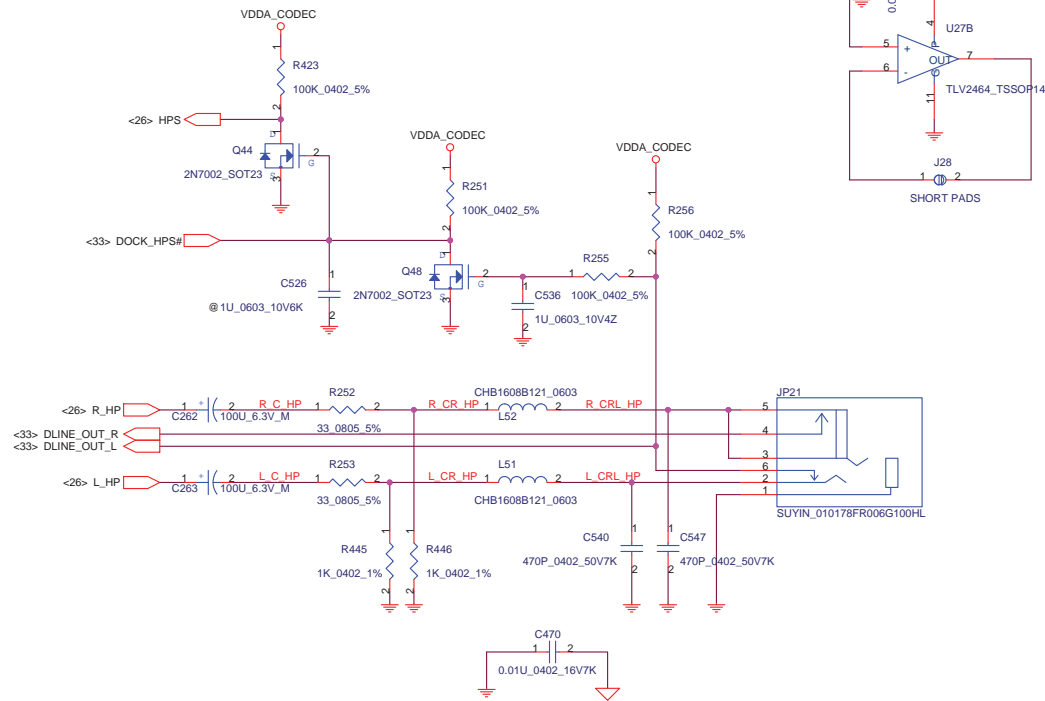
## AMP. FOR INTERNAL MICROPHONE



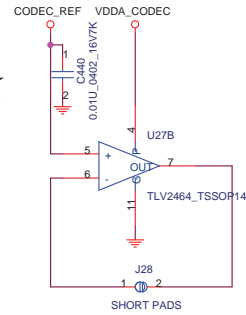
## AMP. FOR EXTERNAL MICROPHONE



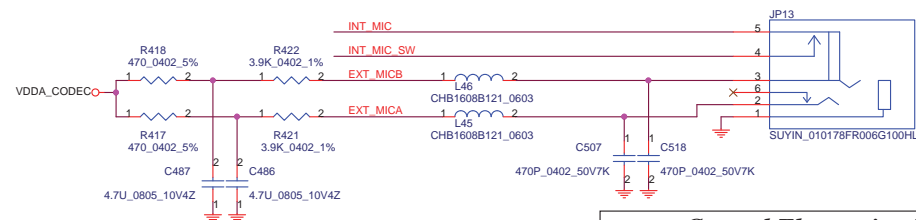
## LINE OUT/HEADPHONES AUDIO JACK



## UNUSED



## EXT. MICIN AUDIO JACK



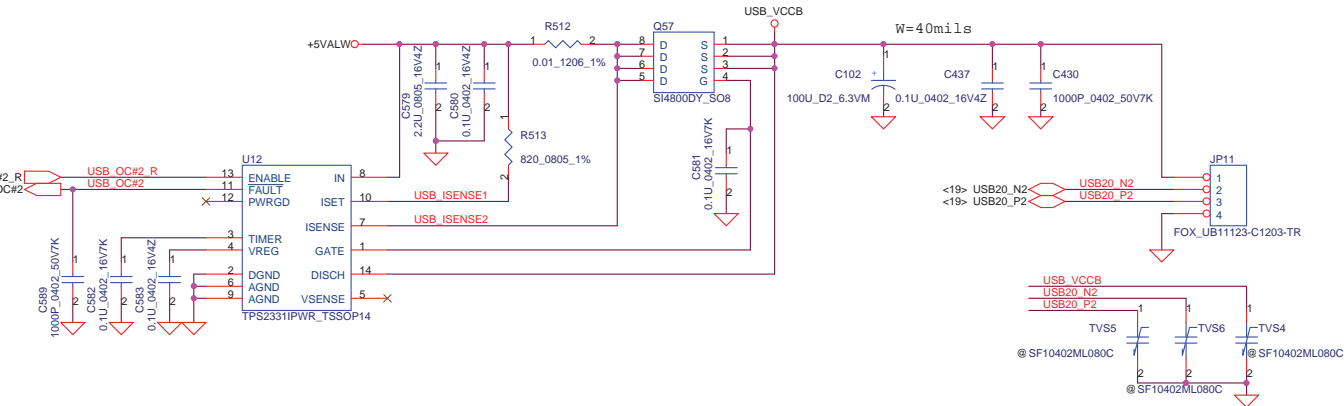
Compal Electronics, Inc.

AMP & Audio Jack

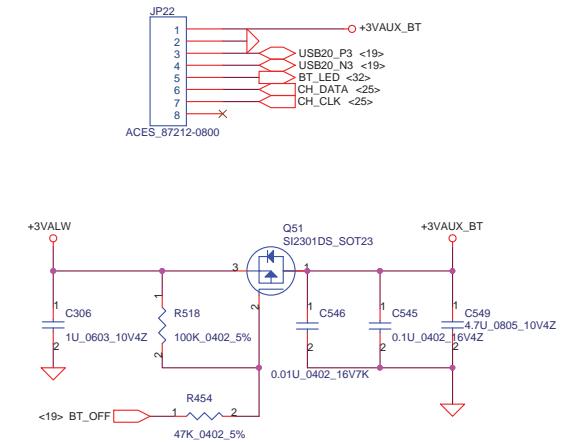
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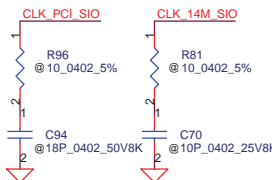
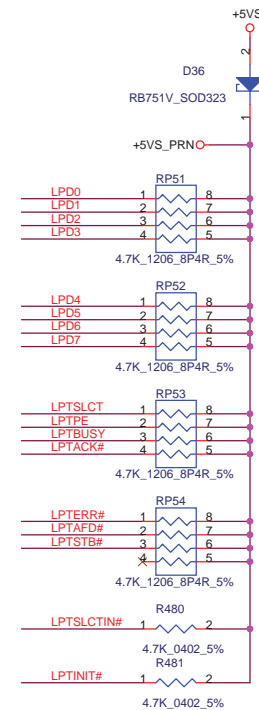
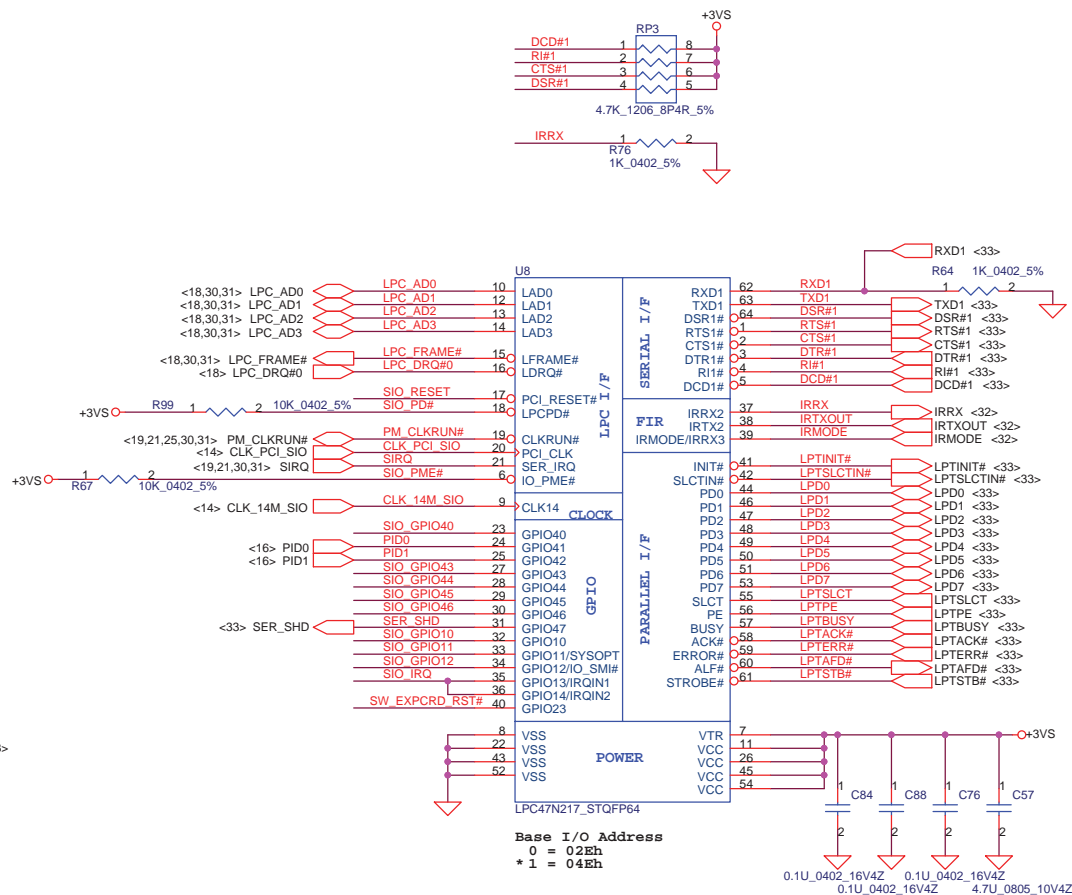
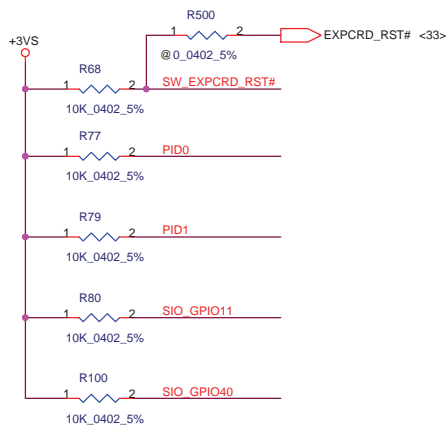
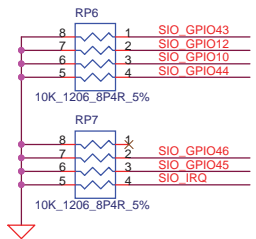
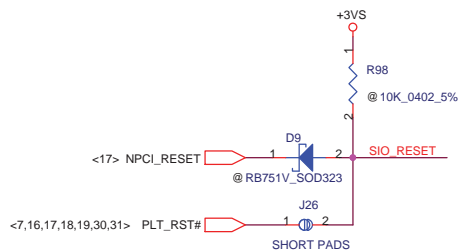
Revision History  
Rev. 0.6  
Date: Thursday, September 09, 2004  
Sheet 27 of 48

### USB CONNECTOR 3



## BT Connector





**BIOS ROM**

The schematic diagram illustrates the BIOS ROM circuit, featuring two integrated circuits (U20 and U21) connected to a +3VS power supply and ground.

**U20 (SST49LF008A-33-4C-El-TOP40) Pin Connections:**

- Address/Data:** A0/ID0 (24), A1/ID1 (23), A2/ID2 (22), A3/ID3 (21), A4/TBL# (20), A5/WP# (19).
- Data:** DQ0/FWH0 (25), DQ1/FWH1 (26), DQ2/FWH2 (27), DQ3/FWH3 (28), DQ4/FWH4 (29).
- Control:** R/C#/CLK (12), RST# (37), OE#/INIT# (38), IC (2).
- Power:** VDD2 (39), VDD1 (10), VSS3 (40), VSS2 (30), VSS1 (29).

**U21 (1M8\_PLCC32) Pin Connections:**

- Address/Data:** LPC AD0 (13), LPC AD1 (14), LPC AD2 (15), LPC AD3 (16), LPC FRAME# (23), FWH WP# (7), FWH TBL# (8), PLT RST# (2), FWH INIT# (24), CLK PCI\_FWH (31).
- Data:** FWH GPIO (6), FWH GP1 (5), FWH GP2 (4), FWH GP3 (3), FWH GP4 (30).
- Control:** RES (21), INIT# (20), ID0 (19), ID1 (18), ID2 (17), IC (29).
- Power:** VDD (25), VDD (32), GND (16), GND (28).

**Other Components and Connections:**

- Capacitors:** C42 (0.1uF, 0402, 16V4Z), C28 (0.1uF, 0402, 16V4Z).
- Resistors:** R273 (100k, 0402, 1%), R274 (100k, 0402, 1%), R275 (100k, 0402, 1%), R276 (100k, 0402, 1%), R277 (100k, 0402, 1%), R278 (10k, 0402, 5%), R279 (10k, 0402, 5%).
- Power Supply:** +3VS connected to VDD pins of U20 and U21.
- Ground:** GND connected to GND pins of U20 and U21.

[illegible]

<16,31,32> KSI\_D\_11 [KSI\_D\_11] 2 SW2 1 KSO15 [KSO15] <31,32>  
X 4 EVQPJT05M\_4P 3 X

<31,32> KSI\_D\_12

KSI\_D\_12

SW1

2 1

KSO15

4 3

EVQPT05M\_4P

3V3V\_LV

D41  
17-21SYGC/S530-E1/TR8\_GRN

R259  
150\_0402\_5%

Q25  
2N7002\_SOT23

STB\_LED#

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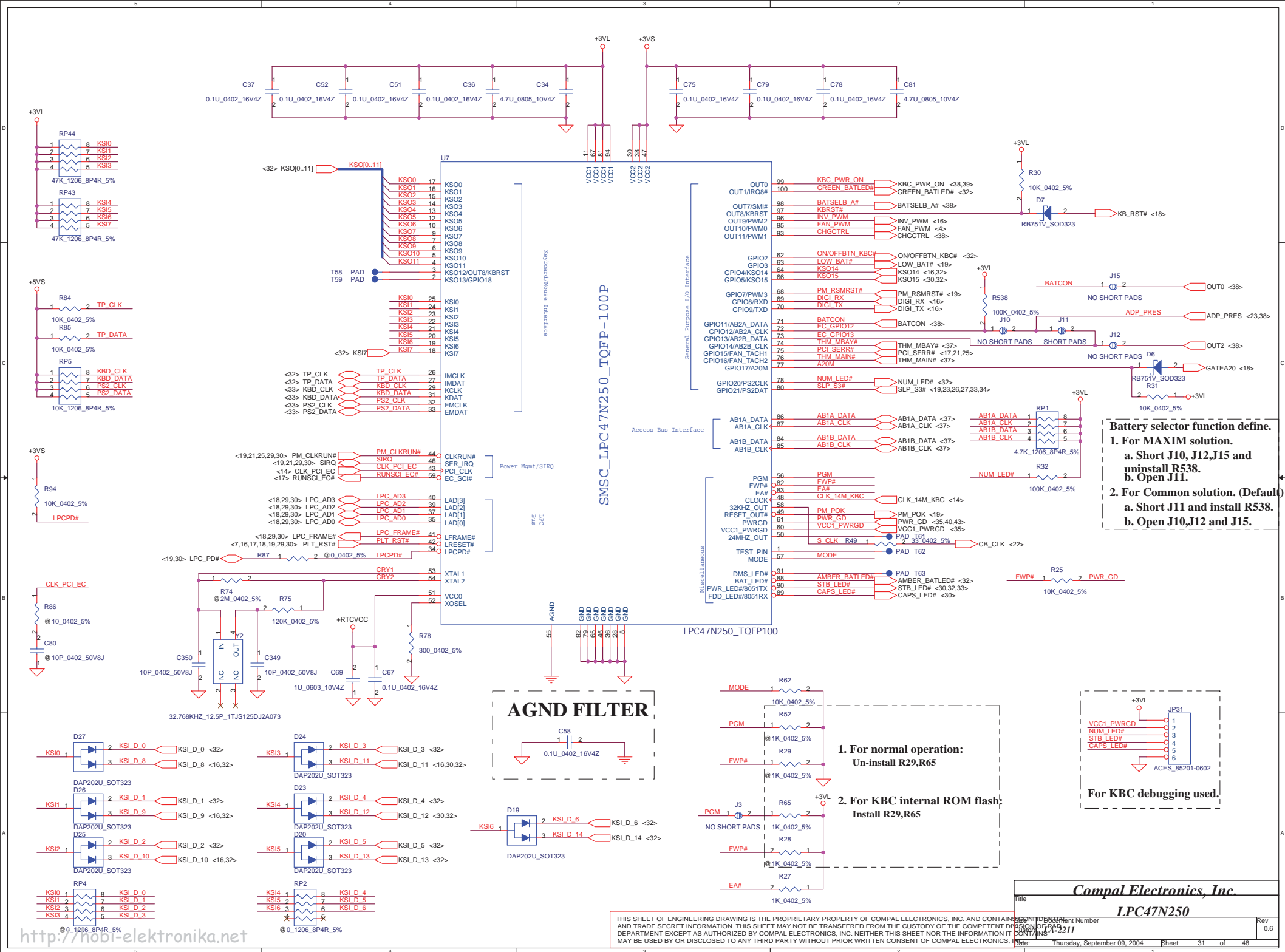
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44

Size: <b>6-A-2211</b> DIVISION OF R&D CUSTOMER:		Rev 0.6
Date: Thursday, September 09, 2004	Sheet 30 of 48	

Rev	
0.6	



The image displays two detailed pinout diagrams for the FUN BD. and FIR & LED BD. boards.

**FUN BD. Pinout:**

- JP9:** A 12-pin header with pins 1-12. Pin 1 is connected to +3VS. Pins 2-12 are connected to various signals: KSI\_D\_8, KSI\_D\_9, KSI\_D\_10, KSI\_D\_13, KSO14, KSO15, LID\_SW#, EAPD#, NUM\_LED#, and ACES\_87212-1200.
- Other Signals:** <16,31> KSO14, <30,31> KSO15, <9,19> LID\_SW#, <27> EAPD#, <31> NUM\_LED#.

**FIR & LED BD. Pinout:**

- JP18:** A 40-pin header with pins 1-40. Pins 1-10 are connected to +3VS, +5VS, +3VALW, +3VALW, +5VS, +3VS, +3VALW, +5VS, +3VS, and +3VLO. Pins 11-40 are connected to various signals: IRRX, IRTXOUT, IRMODE, HDD\_LED#, AMBER\_BATLED#, BT\_LED, WL\_LED, STB\_LED#, PANEL\_FLIP#, GREEN\_BATLED#, and ACES\_85203-2002.
- Other Signals:** <29> IRRX, <29> IRTXOUT, <29> IRMODE, <18> HDD\_LED#, <31> AMBER\_BATLED#, <28> BT\_LED, <25> WL\_LED, <30,31,33> STB\_LED#, <19> PANEL\_FLIP#, <31> GREEN\_BATLED#.

## Power button

The schematic diagram illustrates the power button circuit. It features a 3V\_L power supply connected to a 100K\_0402\_5% resistor (R22) and a 1U\_0603\_10V4Z capacitor (C23). The other end of R22 is connected to the input of a 5V SN74LVC14APWLV\_TSSOP14 inverter (U5F). The output of U5F is connected to a 100K\_0402\_5% resistor (R26) and a 1U\_0603\_10V4Z capacitor (C11). The other end of R26 is connected to the gate of a 2N7002\_SOT23 MOSFET (Q70). The source of Q70 is connected to ground, and the drain is connected to a 3V\_L power supply through a 100K\_0402\_5% resistor (R536). The drain of Q70 is also connected to a 3V\_ALW power supply through a 100K\_0402\_5% resistor (R8) and an RB75TV\_SOD323 diode (D42). The diode D42 is connected to the ON/OFFBTN# signal. The ON/OFF# signal is connected to the input of the inverter U5F. The ON/OFFBTN# signal is also connected to the ON/OFFBTN# signal.

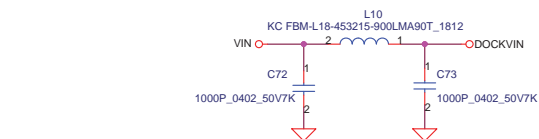
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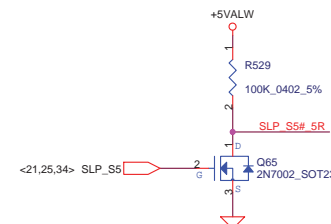
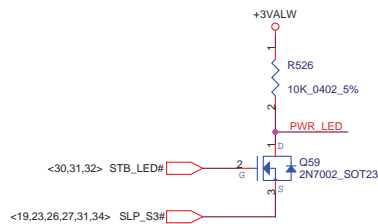
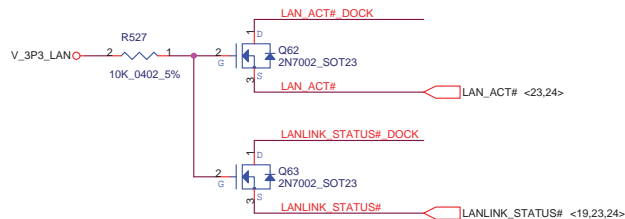
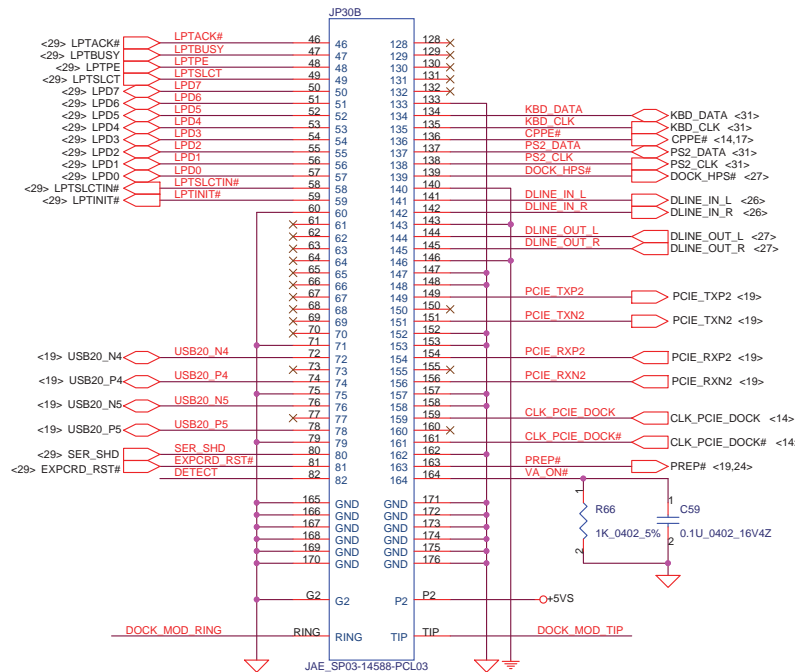
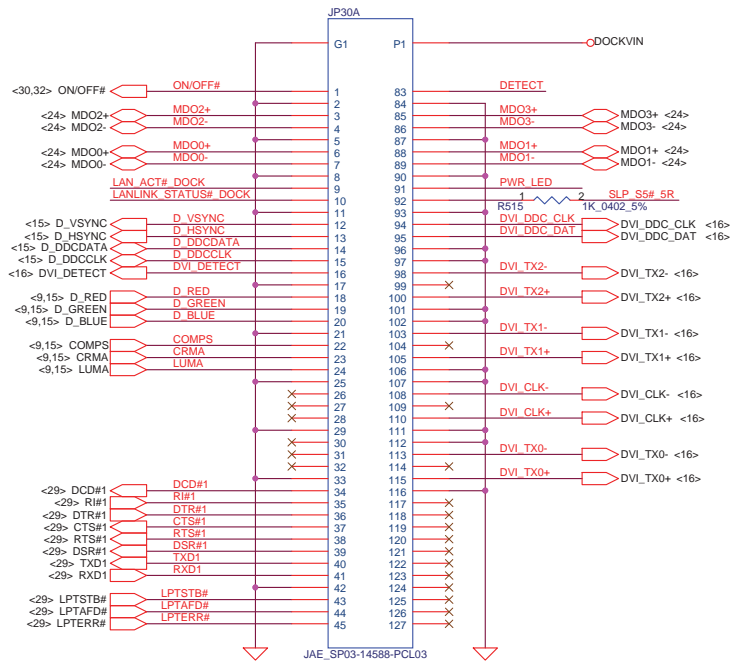
The image contains two circuit diagrams. The left diagram shows a header JP14 (ACES\_87153-0801L) with 8 pins. Pins 1, 3, 5, and 7 are connected to a signal line labeled SP\_DATA. Pins 2 and 4 are connected to a signal line labeled SP\_CLK. Pin 8 is connected to a +5VS power supply. The right diagram shows a header JP17 (ACES\_87212-0800) with 8 pins. Pins 1, 2, and 3 are connected to a signal line labeled TP\_DATA. Pins 4 and 5 are connected to a signal line labeled TP\_CLK. Pins 6 and 7 are connected to a signal line labeled SP\_DATA. Pin 8 is connected to a signal line labeled SP\_CLK. A +5VS power supply is connected to pin 1. There are also two unlabeled signal lines connected to pins 2 and 3.

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<p>Title</p> <p><b>Compal Electronics</b></p>	<p>Document Number</p> <p><b>MDC/KBD/ON (</b></p>
<p>Revision</p> <p><b>LA-2211</b></p>	<p>Date</p> <p><b>Thursday, September 09, 2004</b></p>



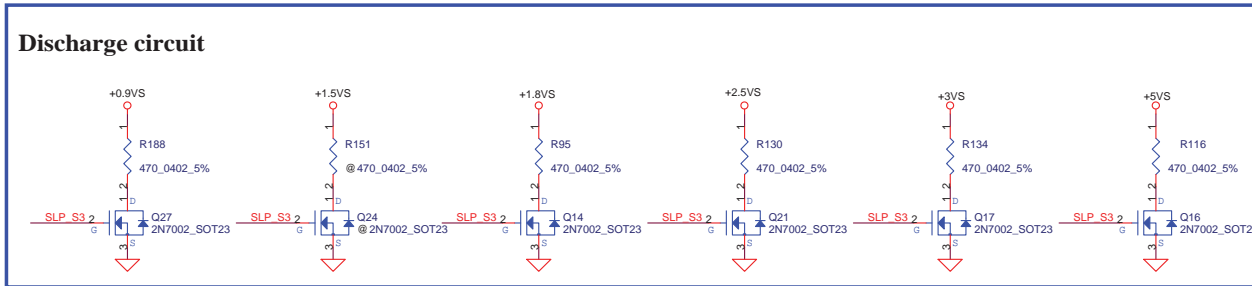
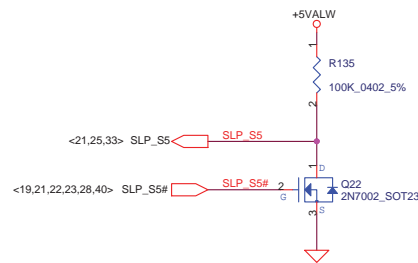
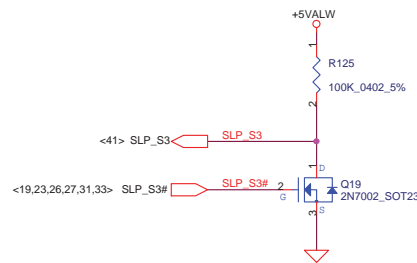
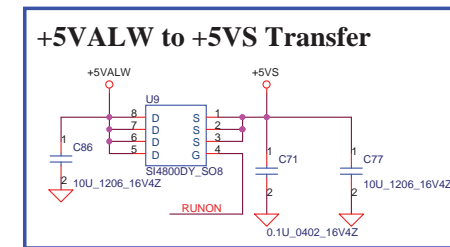
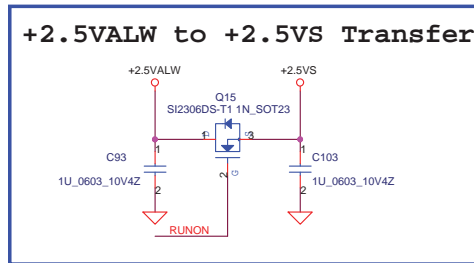
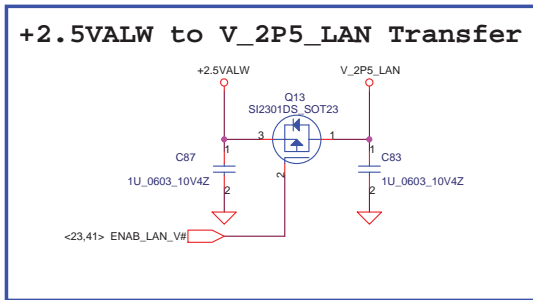
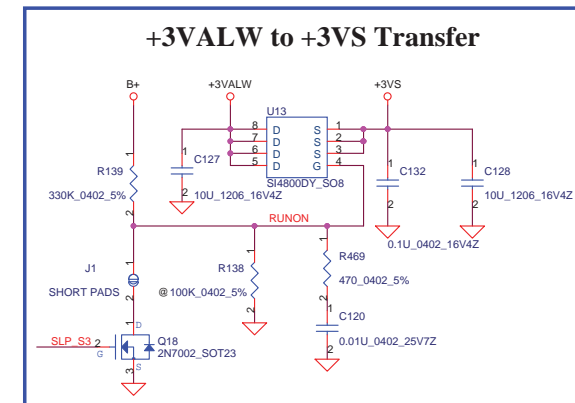
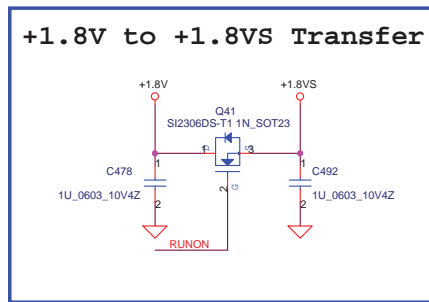
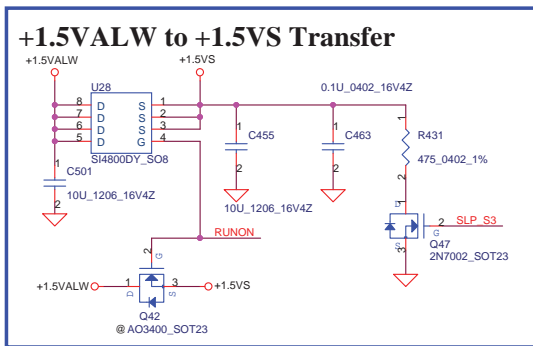


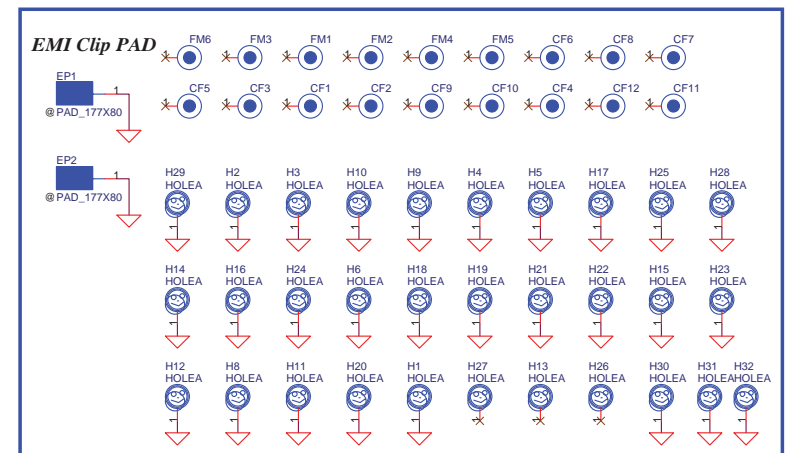
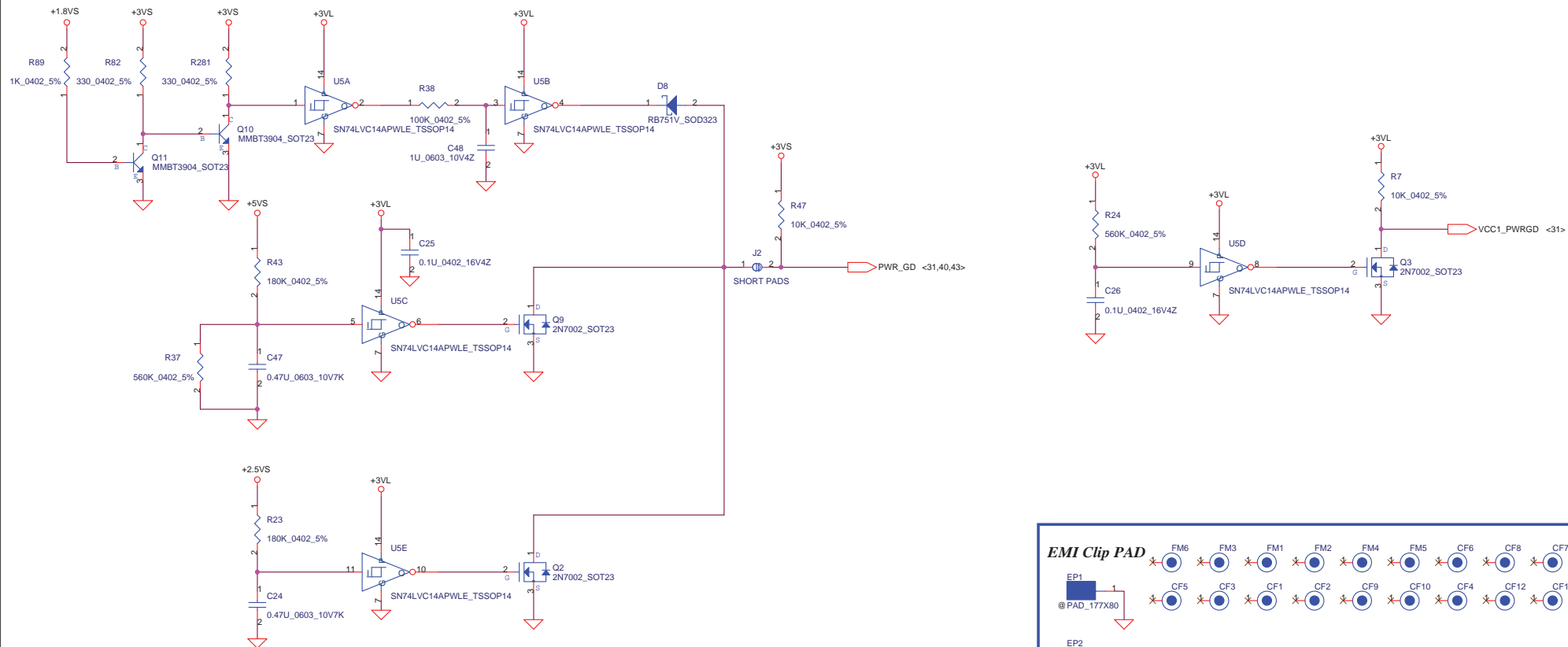
## DOCK CONN. 184PIN



Compal Electronics, Inc.	
SPR Connector	
Title	Revision
Document Number	Rev 0.6
Date	Thursday, September 09, 2004
Sheet	33 of 48

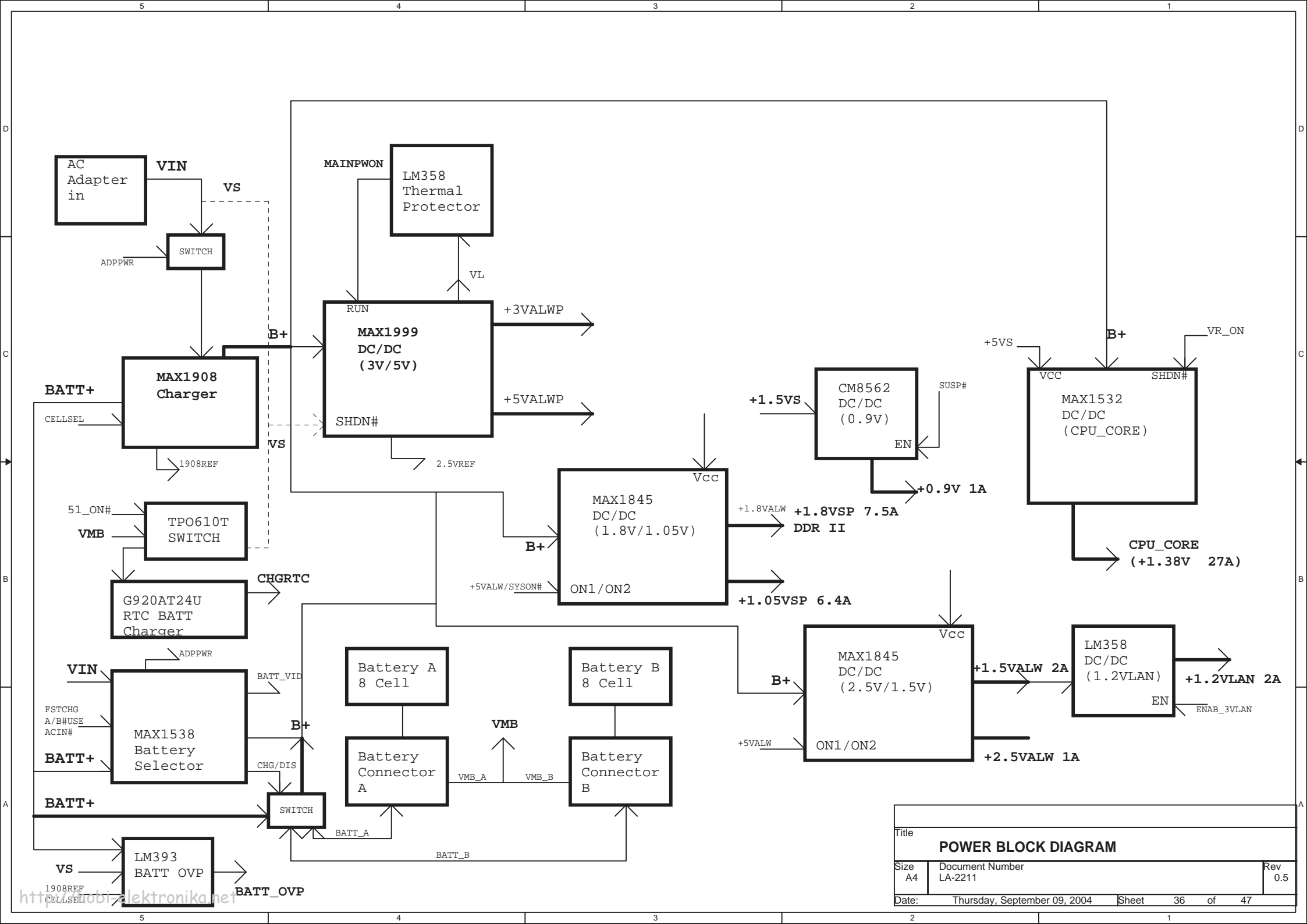
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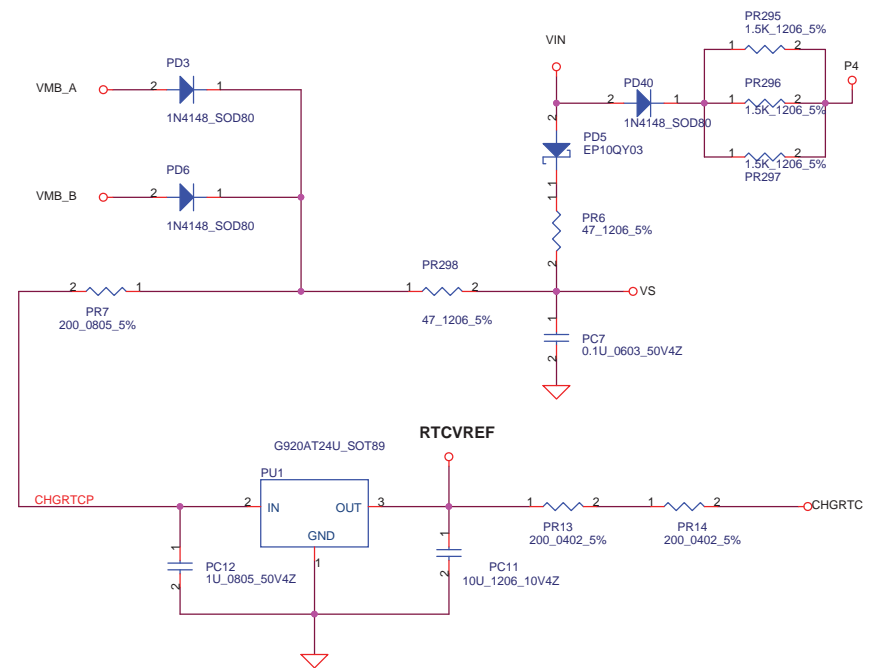
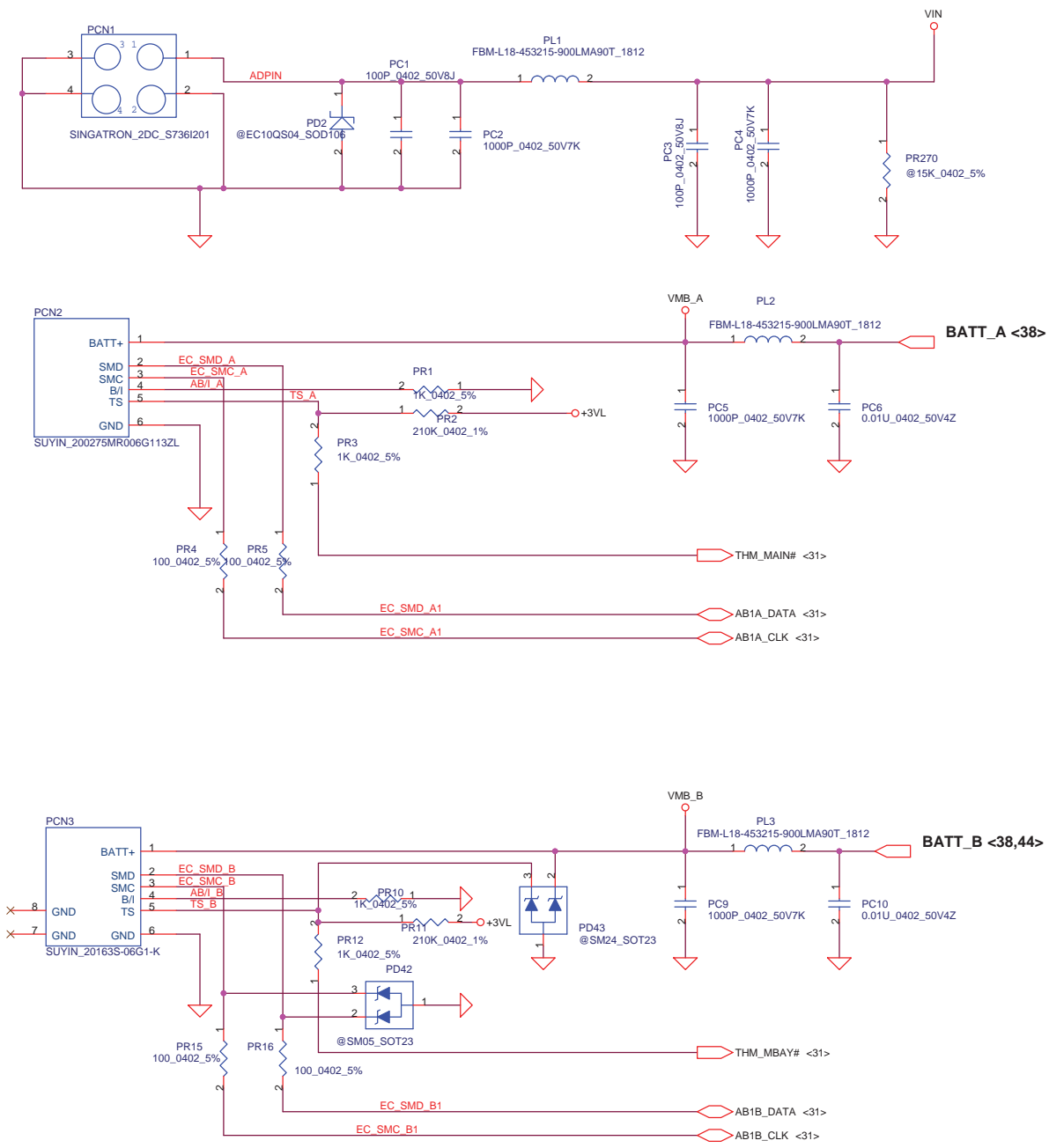


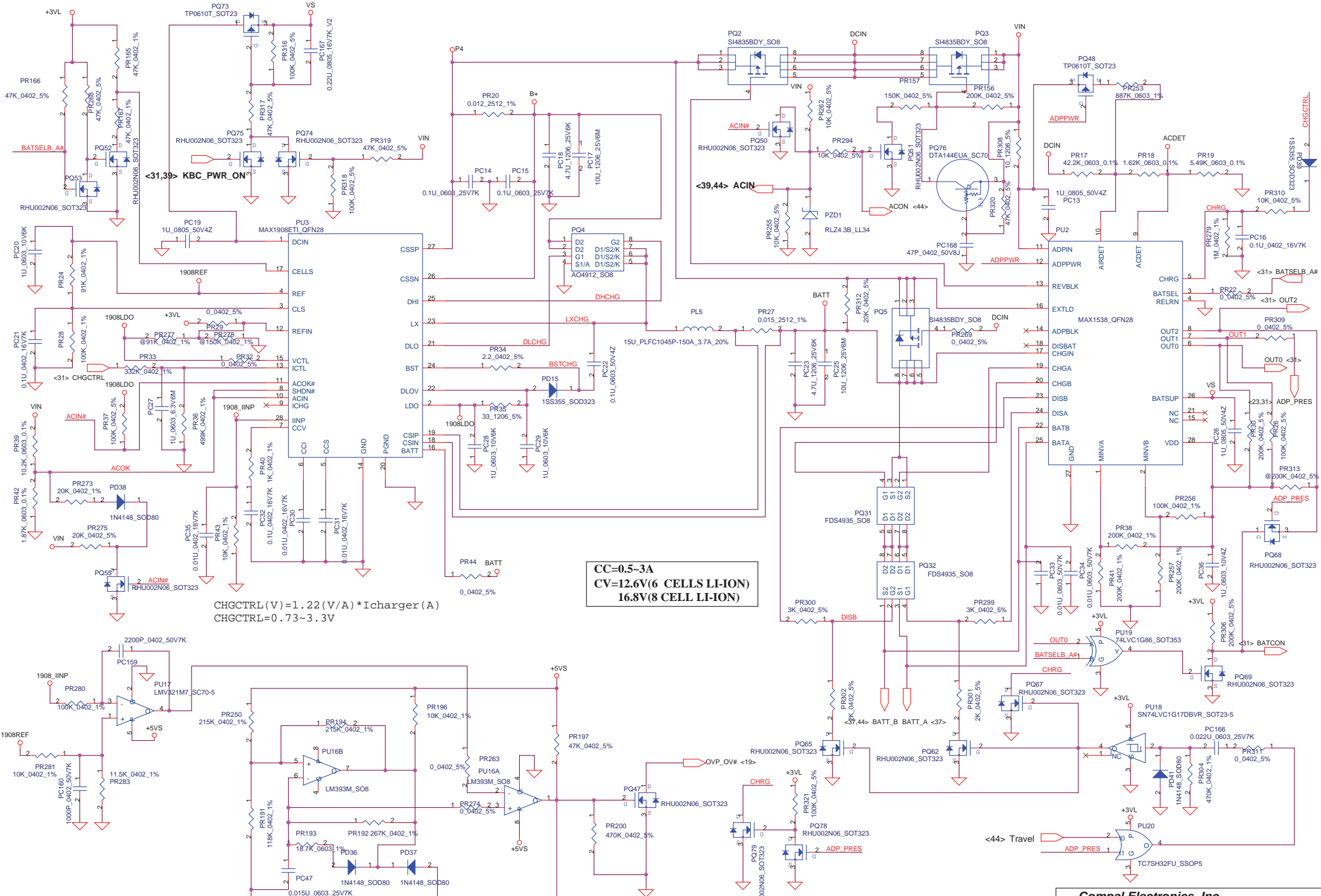
Compal Electronics, Inc.			
Title	POK CKT		
Revision	15-2211	Rev	0.6
Date	Thursday, September 09, 2004	Sheet	35 of 48

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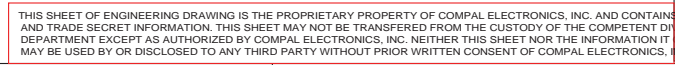
Title		
POWER BLOCK DIAGRAM		
Size	Document Number	Rev
A4	LA-2211	0.5
Date:	Thursday, September 09, 2004	Sheet 36 of 47

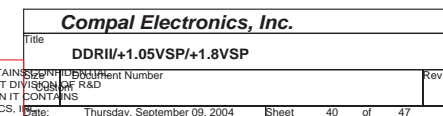




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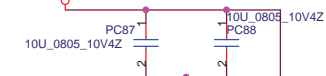
Compal Electronics, Inc.			
Charger			
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Date:	Thursday, September 09, 2004	Sheet	38 of 47



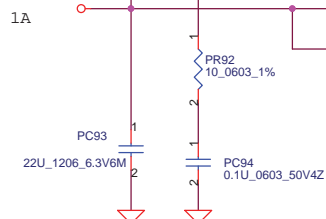




+1.5VS



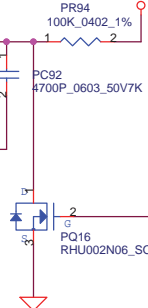
+0.9VSP



+3VS

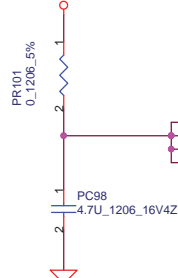


+1.8VP

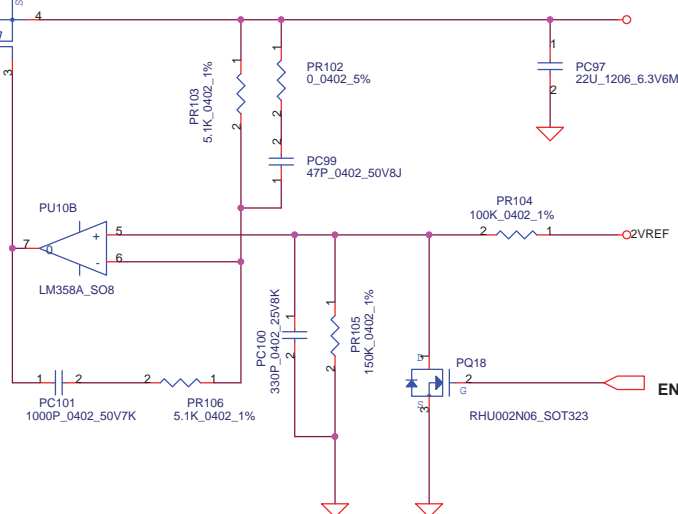


SLP\_S3 <34>

+1.5VALW



+1.2VLANP



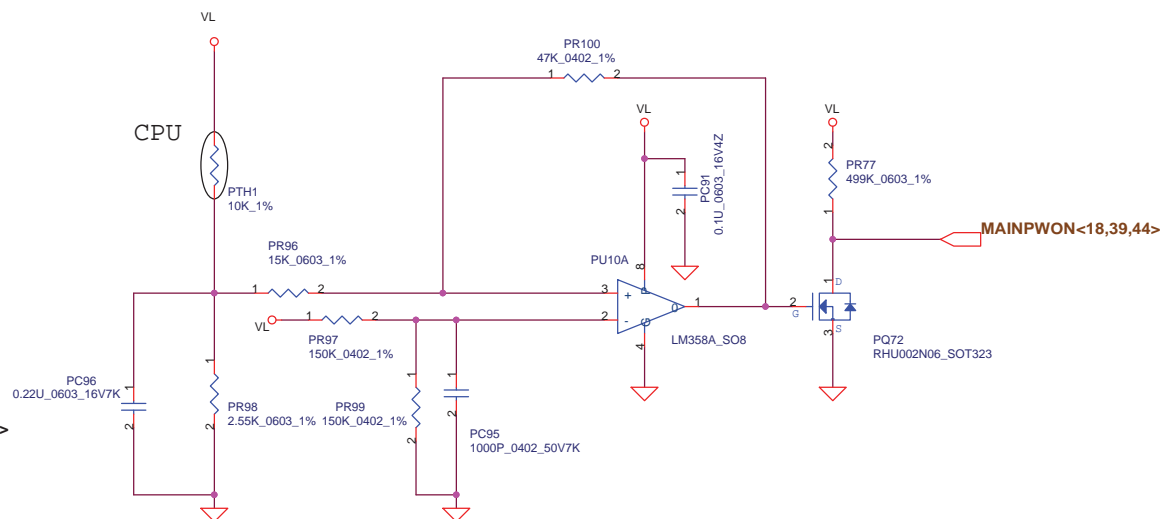
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PH1 under BATT botten side :

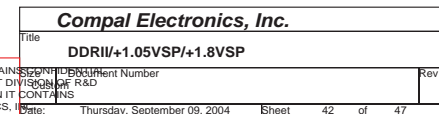
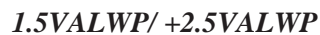
CPU thermal protection at 90 +-3 degree C

Recovery at 43 +-3 degree C

CPU

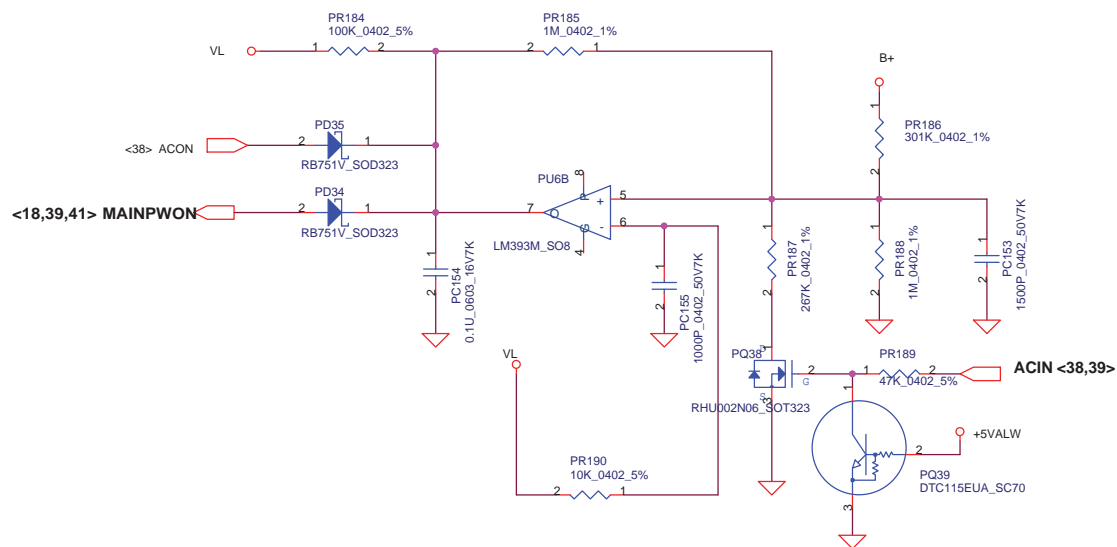


MAINPWON<18,39,44>



<http://hobi-elektronika.net>





## Version Change List ( P. I. R. List ) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	39	12VALWP	03/3/2004 (DB2)	HP	remove 12V	delete PQ11,PC54,PR55,PC42,PR52,PD16,PC41,PR51	DB2
2	41	+1.2VLANP	03/3/2004 (DB2)	Compal	1.2VLANP rise plus voltage	change the Vref form 2.5VREF to 2VREF, and change PR104 form 107k_0603 to 100k_0402, PR105 form 100k_0402 to 150k_0402	DB2
3	44	BATT_OVP	03/3/2004 (DB2)	Compal	For BATT_OVP issue	add PC157,PC158 change PR241 from 20k_0402 to 499k_0402, PR243 from 40.2k_0603 to 402k_0402 , PR244 from 453k_00603 to 4499k_0402, PR251 from 20k_0402 to 499k_0402.	DB2
4	41	+1.2VLANP	03/3/2004 (DB2)	Compal	For ME issue	Change PC97,PC93 from 22u_1210 to 22u_1206	DB2
5	38	CHARGER	03/3/2004 (DB2)	Compal	For Charger issue	Change PC27 from 0.1u_0402 to 1u_0603	DB2
6	38	CHARGER	03/3/2004 (DB2)	HP	For SYSTEM OCP function issue	Delete PR263,PR274 . add PU17,PR280,PR281,PR282,PR283,PC159.	DB2
7	38	CHARGER	03/19/2004 (DB2)	HP	For support that Main Battery is 4 cell pack (4S).	add PQ60,PQ61,PQ62,PR284,PR285,PR286,PR287	DB2
8	38	CHARGER	04/20/2004	HP	To drop the 4 cell battery design.	delete PQ60,PQ62,PR284,PR285,PR287	SI
9	42	1.5VALW/2.5VALW	04/20/2004	Compal	For +1.5VS/+2.5VS peak current issue	Change PL16 from 5uF to 3.3uF PLC0745-3R3A Change PR177 from 100k to 301k Change PR178 from 100K to 0 ohm	SI
10	39	3.3VALW/5VALW	04/28/2004	HP	remove 12V	Change PU7 from MAX1902 to MAX1999 delete PD19,PD20,PR58,PR61,PR63,PR64,PR66,PR59. add PR294,PR295,PR296,PR287,PR288.	SI
11	38	CHARGER	05/13/2004	Compal	add B+ soft start resister.	Add PR294,PR295,PR296	SI
12	38	CHARGER	07/5/2004	HP	For MAX1538 5ms issue	Add PU18,PQ62,PQ65,PD41,PR299, PR300,PR301,PR302,PR304,PR305,PC166	SI1-B
13	38	CHARGER	07/5/2004	HP	Add HP common logic solution	Add PU19,PQ68,PQ69,PR306	SI1-B
14	39	3.3VALW/5VALW	07/5/2004	HP	For S5 POWER consumption issue	Add PQ70,PQ71,PR314	SI1-B
15	38	CHARGER	09/1/2004	HP	remove AC OCP	delete PR249	SI2
16	38	CHARGER	09/1/2004	Compal	To improve S5 POWER consumption	Add PQ73,PQ74,PQ75,PR316,PR317,PR318,PR319,PC167	SI2

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1	26	AGND	03/22/2004 (DB2)	HP	Link AGND and GND with capacitor	changeR460,R461,R462,R463 from 0_0402_5% to C563,C564,C565,C566 0.1U_0402_16V4Z	DB2(0.3)
2	16	SiI1362	03/22/2004 (DB2)	HP	Follow SiI1362 demo circuit	changeR117 from 100_0402_5% to 1k_0402_5% changeR105 from 300_0402_5% to 1k_0402_5%	DB2(0.3)
3	16	SiI1362	03/23/2004 (DB2)	HP	Follow SiI1362 data sheet recommend	Add R493,R494,R495,R496 300_0402_1% Add C567,C568,C569,C570 0.1U_0402_16V4Z	DB2(0.3)
4	27	Microphone circuit	03/23/2004 (DB2)	HP	To improve frequency response	Add L57,L58,L59,L60,L61 HLC0603CSCCR10JT_0603 Add C571,C572,C573,C574,C575 68P_0402_50V8J	DB2(0.3)
5	32	Trackpoint CONN	03/23/2004 (DB2)	Compal	Change trackpoint connector from pitch1.0mm to 0.5mm	change JP14 from ACES_85203-0802 to ACES_87153-0801L	DB2(0.3)
6	23	V_1P2_LAN	04/01/2004 (DB2)	Compal	V_1P2_LAN ripple over spec	change L8,L29,L30,L32,L33 from 0_0603_5% to BLM11A601S_0603	DB2(0.3)
7	4	ADM1031	04/02/2004 (DB2)	Compal	Can't read DDRII temprature	link Q43 pin1 from GND to Q43 pin2	SI1(0.4)
8	23	ATTN_BTTN#	04/08/2004 (DB2)	HP	Per Broadcom, this signal should be pulled up to +3VS.	Delete R72 layout pad and change R73.1 from GND to +3VS.	SI1(0.4)
9	16	CH7307	04/08/2004 (DB2)	CHrontle	Recommendation from Chrontle.	1. Pin25 VSWING for CH7307 should be added 1.2K ohm to GND. 2. Pin 26, 27 should be GND as 10K ohm. 3. Pin3 AS should be pull up as 1K ohm.	SI1(0.4)
10	29,33	SER_SHD	04/08/2004 (DB2)	HP	Add active high signal SER_SHD to GPIO47 on U8 pin 31 that connects to pin 80 on docking connector JP30B. Add Pull down to this signal. This is used to control serial port transceiver in dock.		SI1(0.4)
11	34	PWR on fail	04/19/2004 (DB2)	Compal	System can't boot reliably.	1. Change Q15 from SI2301 to SI2306. 2. Change Q15.2 control signal from SLP_S3 to RUNON. 3. Change R139 from 100K_0402_5% to 330K_0402_5%.	SI1(0.4)
12	29	MAX3243	04/28/2004 (DB2)	Compal	Delete COM port components.	Delete U33,C558,C559,C561,C560,C562,R468,RP50.	SI1(0.4)
13	9	White screen	04/28/2004 (DB2)	Compal	LCD has white screen when system power on or resume from S3/S4.	1. Exchange U35.3 and U35.5 2. Add a 2.2K_0402_5% pull down resistor on U35.2	SI1(0.4)
14	14,19 23,24	LAN PWR down	04/29/2004 (DB2)	HP	Support LAN controller power down feature when LAN cable do not installed.	1. Delete R499 10K_0402_5%. 2. Add R502,R505,R507 0_0402_5%. 3. Delete R15 4.7K_0402_5%. 4. Add U36,U37 SN74LVC1G17DBVR. 5. Add Q54 2N7002. 6. Add C576,C577 0.1U_0402_16V4Z. 7. Add D32 RB751V. 8. Add R503 100K_0402_5%. 9. Add R504 120K_0402_5%. 10. Add R506 10K_0402_5%.	SI1(0.4)

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15	21	TI Flash media IO	04/30/2004 (DB2)	HP	Solve TI Flash media IO work around circuit.	Add D33,D34 RB751V.	SI1(0.4)
16	19	LANLINK_STATUS#	04/30/2004 (DB2)	HP	Change this signal from pin M3 of U26B to pin C25 of U26C.	1. Add R508 10K_0402_5%. 2. Add Q55 2N7002.	SI1(0.4)
17	21,22	Change power rail	05/12/2004 (DB2)	HP	PCMCIA interface don't support S3 or S5 wake up feature.	Change all of components power rail to main power plane.	SI1(0.4)
18	28	USB+PWR switcher	05/21/2004 (DB2)	Compal	Change USB power switcher from MIC2044 to TPS2330.		SI1(0.4)
19	27	Microphone pre-amp	05/26/2004 (DB2)	HP	Per HP's requirement change microphone pre-amp from MAX4492 to TLV2464A.		SI1(0.4)
20	21,22	Change power rail	05/27/2004 (DB2)	HP	Going back and forth for waking up support for PCMCIA interface.	Change all of components power rail to resume power plane.	SI1(0.4)
21	21,22	Change power rail	07/05/2004 (SI1)	HP	PCMCIA interface don't support S3 or S5 wake up feature.	1. Reserved some component layout pads for +3V/+5V. 2. Add R530 and R537 for supportting PCMCIA power rail with main power rail.	SI1-B(0.5)
22	19,31 32,35	S5 power consumption	07/05/2004 (SI1)	HP	To reduce power consumption on S5. The specification is under 50 mW.	1. Add isolation circuit. (R532,R533,D37,D38) 2. Change some component's power rail from +3VALW to +3VL (R223,R218[V_3P3_LAN],U7,RP44,RP43,R65,R28,R27,JP31 RP1,R32,R31,R30,U5,R22,R24,R7)	SI1-B(0.5)
23	28	USB+PWR switcher	07/20/2004 (SI1)	Compal	To solve voltage droop issue when cradle plugged in USB port.	1. Change C582 from 1000pF to 0.1uF. 2. Add C581 0.1uF. 3. Change C102 to 100uF Low ESR capacitor.	SI2(0.6)
24	31	Wrong voltage level on FWP#.	07/22/2004 (SI1)	Compal	To solve wrong voltage on FWP# when system is powered off.	Delete R28.	SI2(0.6)
25	27	OTS#133751	07/22/2004 (SI1)	Compal	When mute is off, the mute button LED remains on (very dim though).	Change R430 from 100K ohm to 10K ohm.	SI2(0.6)
26	18	ICH_RTCRST# timing	07/22/2004 (SI1)	Intel	Intel changed component's value.	1. Change R230 from 180K ohm to 20K ohm. 2. Change C287 from 0.1uF to 1uF.	SI2(0.6)
27	14	R511	08/03/2004 (SI1)	Compal	For supporting CY28442 on SI2.	Delete R511.	SI2(0.6)
28	27	R429, C504	08/03/2004 (SI1)	HP	Follow Lloyd Daniel's suggestion, change R429 to 16.2K ohm and change C504 to 0.22uF.	change R429 to 16.2K ohm and change C504 to 0.22uF.	SI2(0.6)
29	30	Power LED active error.	08/03/2004 (SI1)	Compal	Swap D41.1 with D41.4 for solving LED active error on SI1-B unit.		SI2(0.6)
30	16,26 32	Modify EMI solution	08/03/2004 (SI1)	Compal		1. Add FBM-L11-201209-221LMAT on L62 and delete R466. 2. Add 0.1u (C586) / 68p (C587) capacitors at B+_LCD. 3. Add CHB2012U121 on L36. 4. Remove CPL~CP7	SI2(0.6)
31	30	Delete sleep button function	08/10/2004 (SI1)	HP	Sleep LED is no longer required.	Delete D40 & R261.	SI2(0.6)
32	30	Add additional R & LED for CAP. function	08/10/2004 (SI1)	Compal	For solving CAP LED bright issue. This requirement was coming from ME team.	1. Add R541 150 ohm. 2. Add green LED 17-21SYGC/S530-E1/TR8.	SI2(0.6)

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33	30	Power Button	08/10/2004 (SI1)	Compal	Change powr button from 2-way to 1-way.	From SS056-Pt213BBT-PA2 to SS607-212N-FEEG1T.	SI2(0.6)
34	19	OTS#137561	08/19/2004 (SI1)	Compal	I found this issue was caused by ICH_PCIE_WAKE# signal generated again. Because V_3P3_LAN disappeared before +3VALW under battery mod. This is wrong.	1. Change R532 from 10K ohm to 1K ohm. 2. Delete D37. 3. Add a additional MOS Q71 (BSS138). 4. Connection Q71.2 with V_3P3_LAN. 5. Connection Q71.3 with D37.1. 6. Connection Q71.1 with D37.2.	SI2(0.6)
35	15	RGB rise/fall time.	08/23/2004 (SI1)	Compal	RGB rise/fall time out of specification issue.	Short L54,L55,L56.	SI2(0.6)
36	18	RTC Accuracy	08/27/2004 (SI1)	Compal	To improve RTC accuracy.	1. Change Y4 to 32.768 KHz +-10 ppm. 2. Change C516 and C528 to 18pF.	SI2(0.6)
37	16	DVI CKT	08/31/2004 (SI1)	HP	Remove any components that associate with Silicon Image controller for DVI.		SI2(0.6)
38	4	ADM1032	09/02/2004 (SI1)	Compal	Change thermal sensor to ADM1032 and reserve a thermal sensor CKT (MAX6646) on page 8.		SI2(0.6)